

MODEL NAME : *DDP00*  
*DDB00*

PCB NO : *LA-G341P*

BOM P/N :

# Dell/Compal Confidential

## Schematic Document

### Superveloce

#### (Berlinetta CFL 4-Phase Design)

2018-05-10

Rev: Pilot A00

@ : Nopop Component

XDP@ : Nopop Component

CONN@ : Connector Component

TPM@ : TPM funct i on

EMC@ : Pop of EMI parts

VRAMS@ : Samsung GDDR5

VRAMM@ : Micron GDDR5

G0VRAMH@: Samsung GDDR5 for G0-GPU

NDS@@ : Nopop Component

N18PQ1@ : GPU N18PQ1

N18PQ3@ : GPU N18PQ3

N17PG0@ : GPU N17PG0

N17PG1@ : GPU N17PG1

UMA@ : UMA

DIS@ : DIS

UMAP@ : UMA for Presist i on

UMAX@ : UMA for XPS

3PHASEPCB@ : PCB for 3Phase

4PHASEPCB@ : PCB for 4Phase

3PHASE@ : PCB for 3Phase

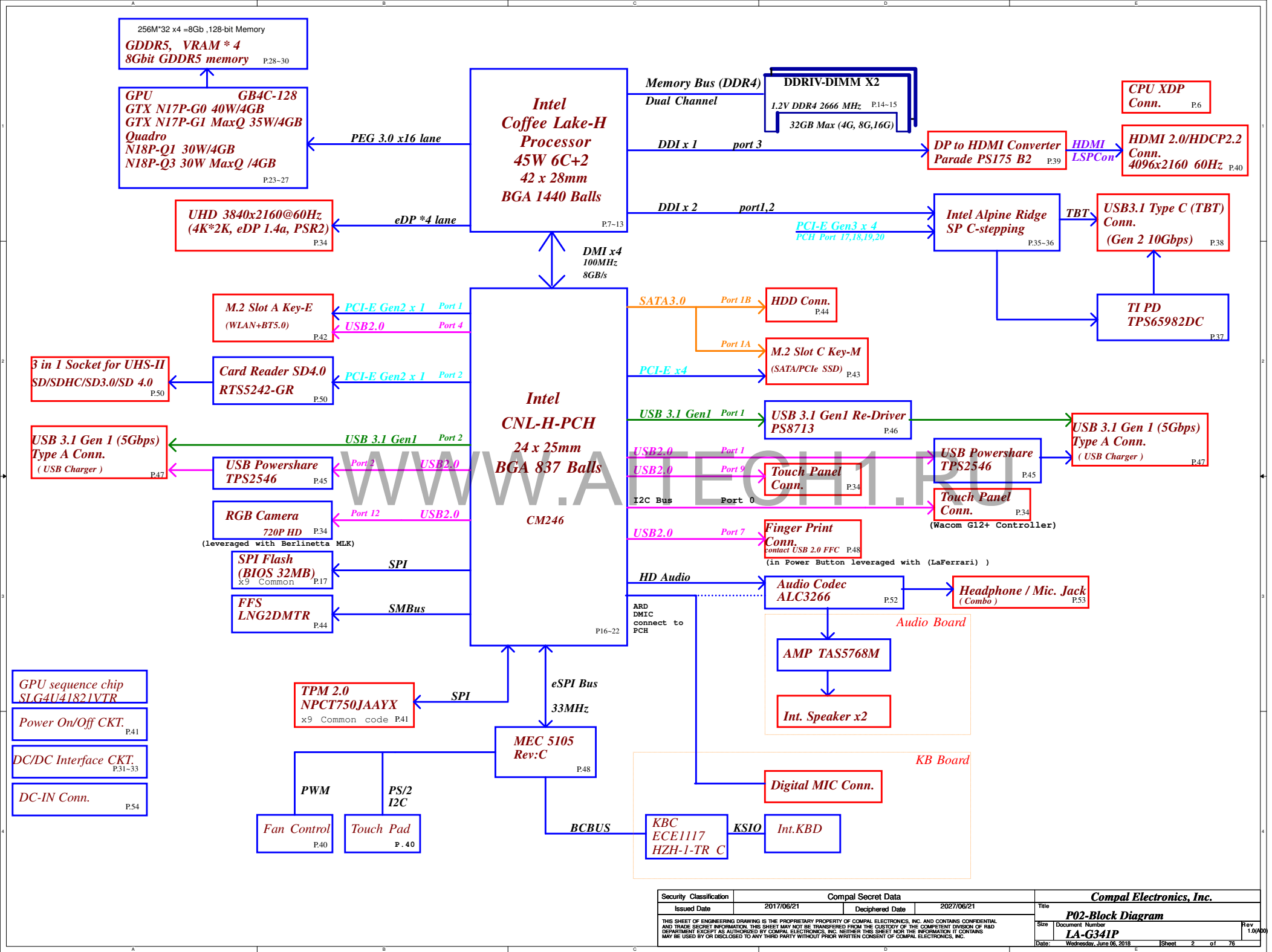
4PHASE@ : PCB for 4Phase

VPRO@ : For VPRO SKU

NVPRO@ : For No-VPRO SKU

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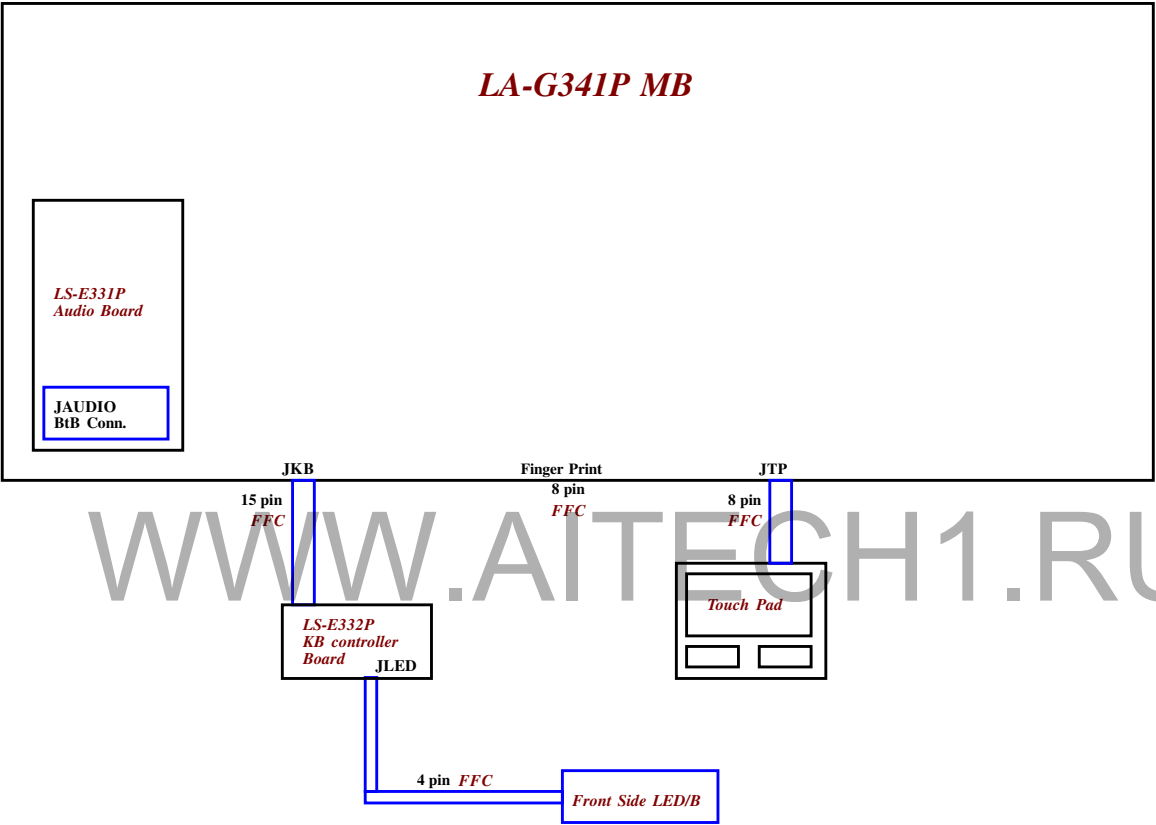
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2017/06/21	Deciphered Date	2027/06/21	Title	<b>P01-Cover Page</b>
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				Date	Rev
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Project Code : DDP00 / DDB00

File Name :



Board ID	Resistor
X00	4.3K
X01	2K
X02	
X03	
A00	1K

USB3.1	DESTINATION
1	USB Conn 1 (Right Side)
2	USB Conn 2 (Left Side)
3	None
4	None
5	None
6	None

USB 2.0	DESTINATION
1	USB Conn 1 (Right Side)
2	USB Conn 2 (Left Side)
3	None
4	NGFF-1 WLAN + BT
5	None
6	None
7	Finger Print
8	None
9	Touch Screen
10	None
11	None
12	RGB CAMERA

USB OC#	DESTINATION
0	USB Conn 1 (Right Side)
1	USB Conn 2 (Left Side)
2	
3	
4	
5	
6	
7	

PCI EXPRESS	DESTINATION	USB3.0	DESTINATION
Lane 1	NGFF-1 WLAN + BT	7	None
Lane 2	None	8	None
Lane 3	None	9	None
Lane 4	None	10	None
Lane 5	CARD READER		
Lane 6	None		
Lane 7	None		
Lane 8	None		
Lane 9	SSD		
Lane 10	SSD	SATA	DESTINATION
Lane 11	SSD	0A	N/A
Lane 12	SSD	1A	SSD
Lane 13	None	0B	N/A
Lane 14	None	1B	N/A
Lane 15	None	2	HDD
Lane 16	None	3	N/A
Lane 17	Alpine Ridge	4	N/A
Lane 18		5	N/A
Lane 19			
Lane 20			

DDI	DESTINATION
1	Alpine Ridge
2	Alpine Ridge
3	HDMI 2.0

LPC	DESTINATION
ESPI/LPC0	MEC5105
LPC1	DEBUG PORT

CLKOUT_PCIE	DESTINATION	CLKOUT_PCIE	DESTINATION
0	None	10	None
1	None	11	None
2	None	12	None
3	NGFF-1 WLAN	13	None
4	CARD READER	14	None
5	Thunderbolt	15	None
6	NGFF-2 SSD		
7	GPU		
8	None		
9	None		

Flex I/O Lane	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29
High Speed I/O (HSIO) Type and Lane	USB3.1 #1	USB3.1 #3	USB3.1 #4	USB3.1 #5	USB3.1 #6	USB3.1 #7	USB3.1 #8	USB3.1 #9	USB3.1 #10	PCIe #1	PCIe #2	PCIe #3	PCIe #4	PCIe #5	PCIe #6	PCIe #7	PCIe #8	PCIe #9	PCIe #10	PCIe #11	PCIe #12	SATA 0a	SATA 0b	SATA 1a	SATA 1b	SATA 2	SATA 3	SATA 4	SATA 5	
Intel® RST Support										No Support	No Support				Yes				No Support		Yes						Yes			

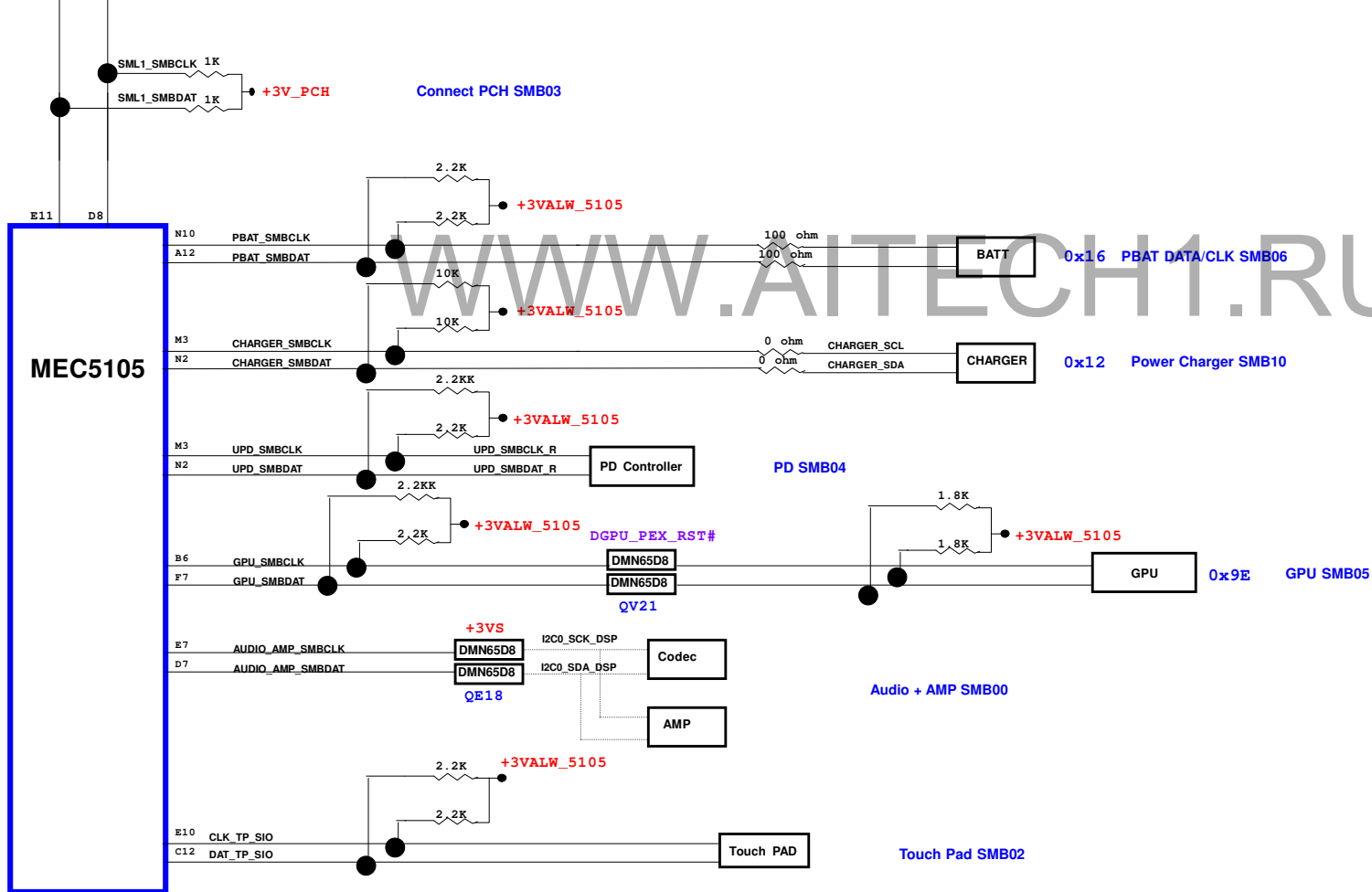
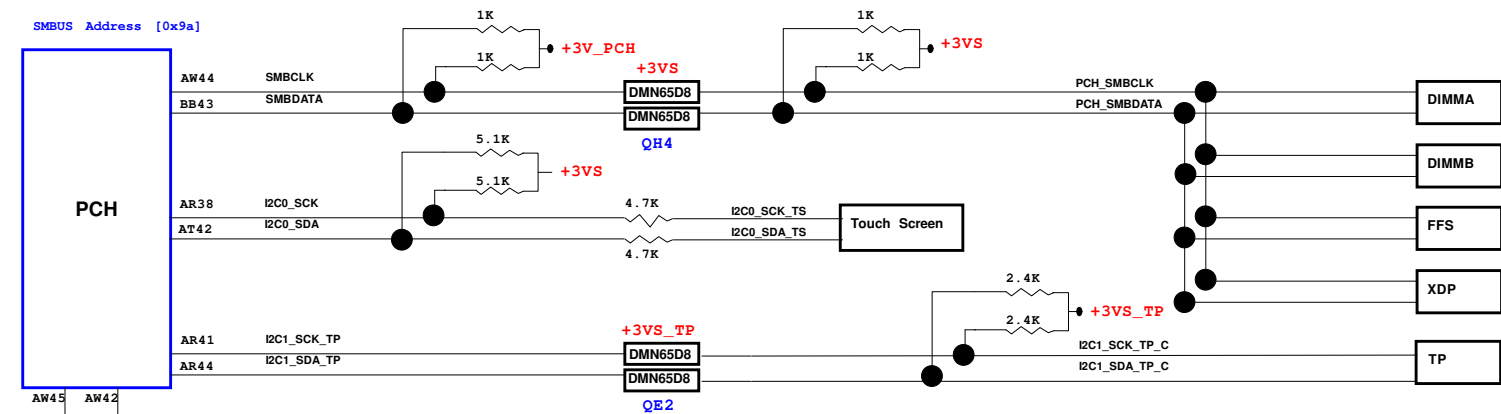
The 30 HSIO lanes on PCB-H supports the following configurations:

- Up to 24 PCIe® Lanes
  - A maximum of 16 PCIe® Ports (or devices) can be enabled
  - When a QoS Port is enabled, the maximum number of PCIe® Ports (or devices) that can be enabled reduces based off the following:
    - Max PCIe® Ports (or devices) = 16 - QoS (0 or 1)
    - PCIe® Lanes 1-4 (PCIe® Controller #1), 5-8 (PCIe® Controller #2), 9-12 (PCIe® Controller #3), 13-16 (PCIe® Controller #4), 17-20 (PCIe® Controller #5), and 21-24 (PCIe® Controller #6) can be individually configured
- Up to 6 SATA Lanes
  - A maximum of 6 SATA Ports (or devices) can be enabled
  - SATA Lane 0 has the flexibility to be mapped to Flex I/O Lane 16 or 18
  - SATA Lane 1 has the flexibility to be mapped to Flex I/O Lane 17 or 19
- Up to 10 USB 3.1 Lanes
  - A maximum of 10 USB 3.1 Ports (or devices) can be enabled
- Up to 4 QoS Lanes
  - A maximum of 1 QoS Port (or device) can be enabled
- Supports up to 3 Remapped (Intel® Rapid Storage Technology) PCIe® storage devices
  - #2 and #4 PCIe® NVMe SSD
  - #2 Intel® Optane® Memory Device
  - See the "PCI Express® (PCIe®)" chapter for the 8 CH PCIe® Controllers configuration
- For unused SATA/PCIe® Combo Lanes, Flex I/O Lanes that can be configured as PCIe® or SATA, the lanes must be statically assigned to SATA or PCIe® via the SATA/PCIe Combo Port Software discussed in the SPI Programming Guide and through the Intel® Flash Image Tool (FIT) tool.

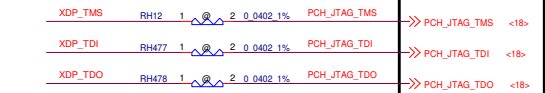
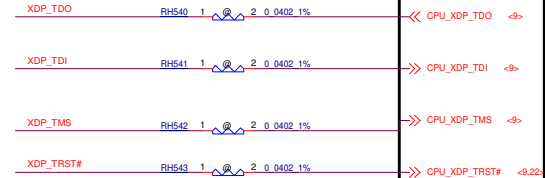
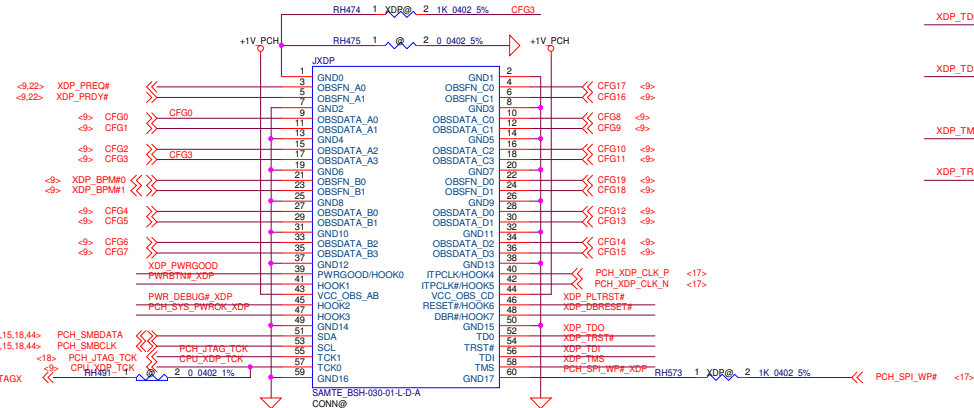
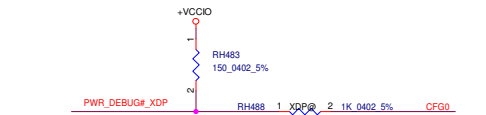
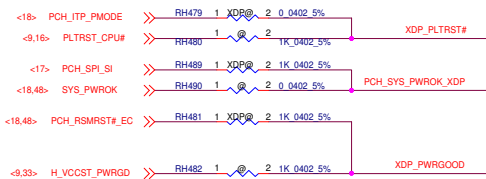
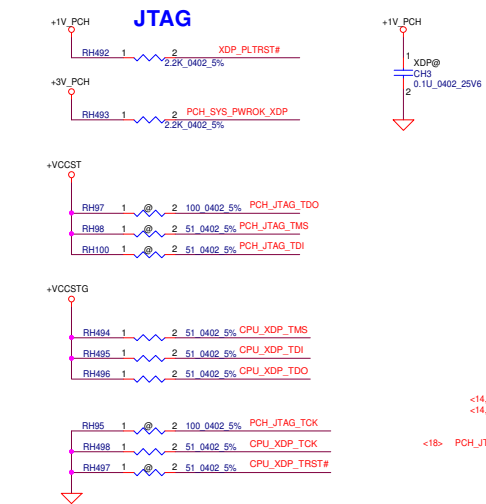
Symbol Note :

↓ : means Digital Ground      ⏏ : means Analog Ground

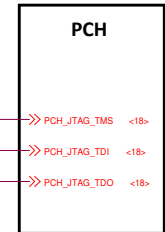
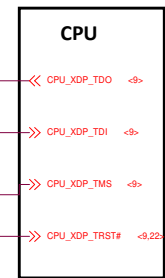
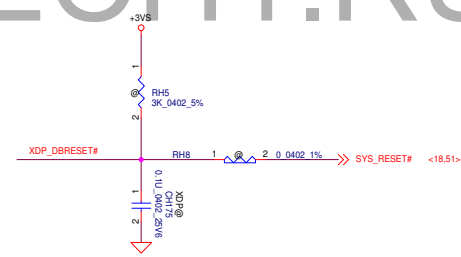
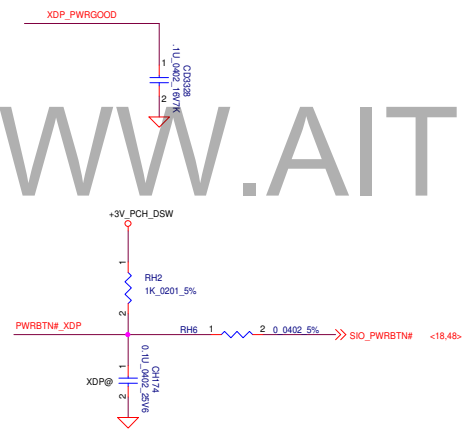




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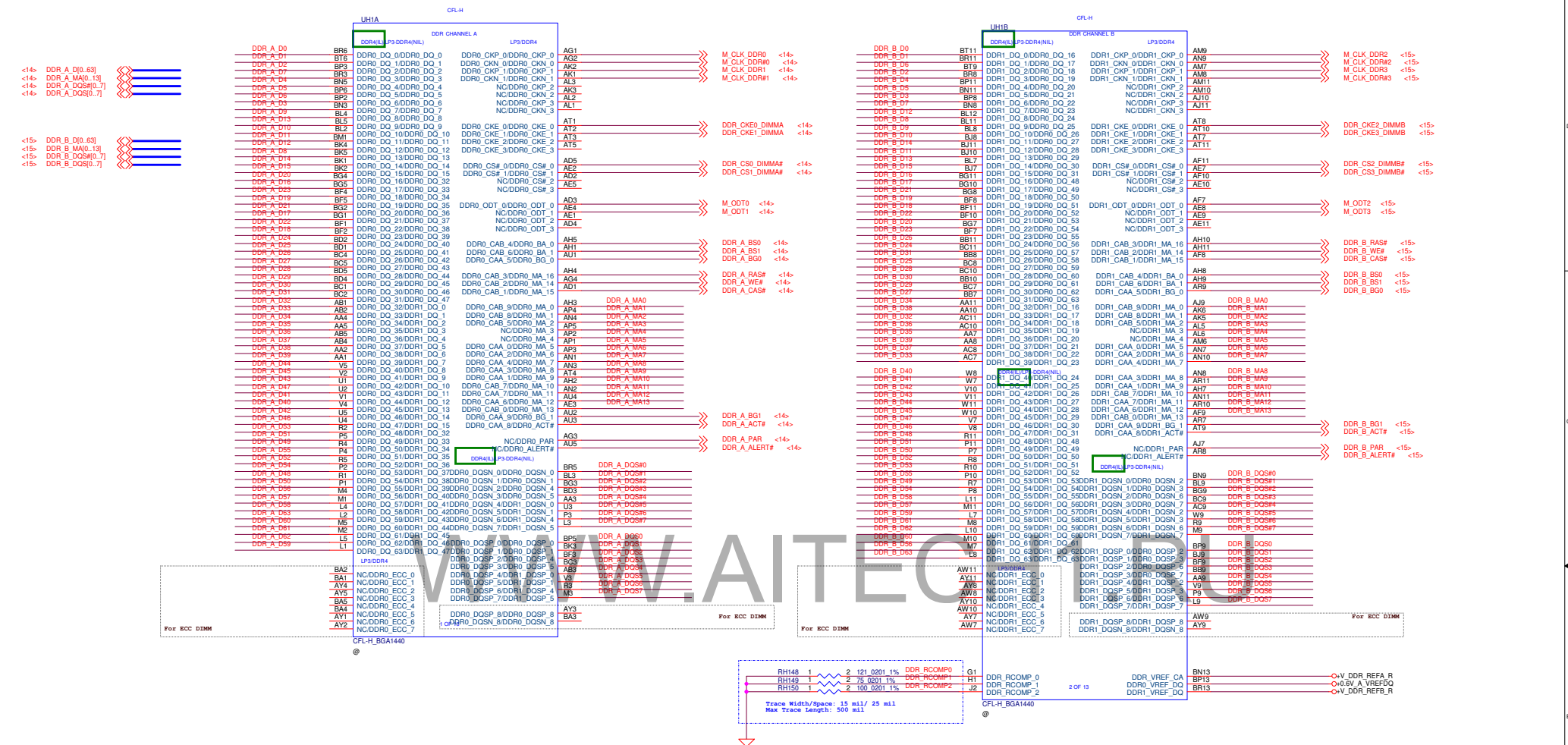
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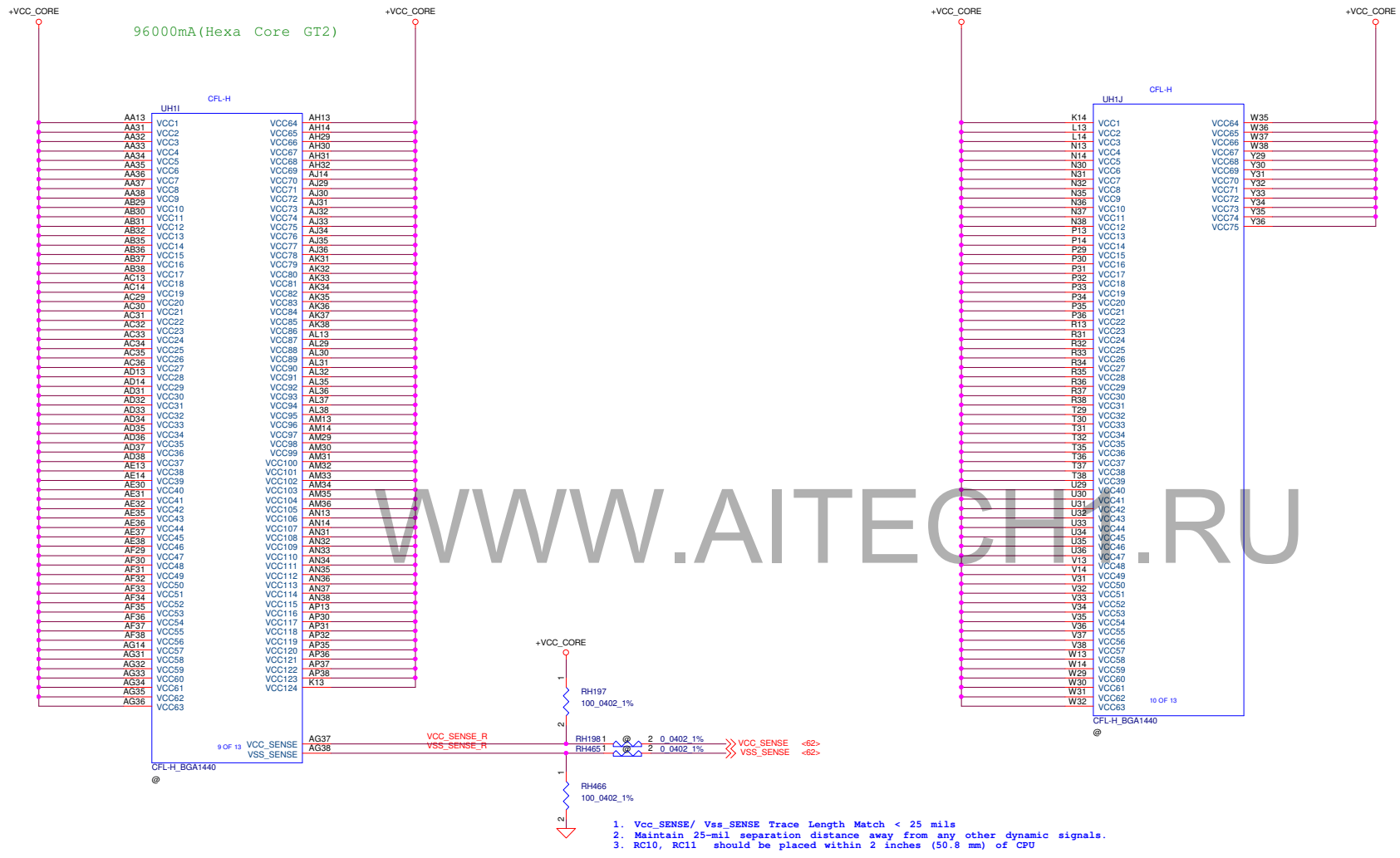
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Size	Document Number	Rev	1.0/000	Date: Wednesday, June 06, 2018
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# Interleave











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1. VccGT\_SENSE / VssGT\_SENSE Trace Length Match < 25 mils
2. Maintain 25-mil separation distance away from any other dynamic signals.
3. RC12, RC13 should be placed within 2 inches (50.8 mm) of CPU

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				Size Custom
				Document Number
				Rev 1.0(A00)
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				Sheet 12 of 76



CFL-H		
UH1F		
A10	VSS_1	VSS_82
A12	VSS_2	VSS_83
A16	VSS_3	VSS_84
A18	VSS_4	VSS_85
A20	VSS_5	VSS_86
A22	VSS_6	VSS_87
A24	VSS_7	VSS_88
A26	VSS_8	VSS_89
A28	VSS_9	VSS_90
A30	VSS_10	VSS_91
A6	VSS_11	VSS_92
A9	VSS_12	VSS_93
AA12	VSS_13	VSS_94
AA29	VSS_14	VSS_95
AA30	VSS_15	VSS_96
AB33	VSS_16	VSS_97
AB34	VSS_17	VSS_98
AB6	VSS_18	VSS_99
AC1	VSS_19	VSS_100
AC12	VSS_20	VSS_101
AC2	VSS_21	VSS_102
AC3	VSS_22	VSS_103
AC37	VSS_23	VSS_104
AC38	VSS_24	VSS_105
AC4	VSS_25	VSS_106
AC5	VSS_26	VSS_107
AC6	VSS_27	VSS_108
AD10	VSS_28	VSS_109
AD11	VSS_29	VSS_110
AD29	VSS_30	VSS_111
AD30	VSS_31	VSS_112
AD6	VSS_32	VSS_113
AD8	VSS_33	VSS_114
AD9	VSS_34	VSS_115
AE33	VSS_35	VSS_116
AE34	VSS_36	VSS_117
AE6	VSS_37	VSS_118
AF1	VSS_38	VSS_119
AF12	VSS_39	VSS_120
AF13	VSS_40	VSS_121
AF14	VSS_41	VSS_122
AF2	VSS_42	VSS_123
AF3	VSS_43	VSS_124
AF4	VSS_44	VSS_125
AG10	VSS_45	VSS_126
AG11	VSS_46	VSS_127
AG13	VSS_47	VSS_128
AG29	VSS_48	VSS_129
AG30	VSS_49	VSS_130
AG6	VSS_50	VSS_131
AG7	VSS_51	VSS_132
AG8	VSS_52	VSS_133
AH12	VSS_53	VSS_134
AH33	VSS_54	VSS_135
AH34	VSS_55	VSS_136
AH35	VSS_56	VSS_137
AH36	VSS_57	VSS_138
AH6	VSS_58	VSS_139
AJ1	VSS_59	VSS_140
AJ13	VSS_60	VSS_141
AJ2	VSS_61	VSS_142
AJ3	VSS_62	VSS_143
AJ37	VSS_63	VSS_144
AJ38	VSS_64	VSS_145
AJ4	VSS_65	VSS_146
AJ5	VSS_66	VSS_147
AJ6	VSS_67	VSS_148
W4	VSS_68	VSS_149
W5	VSS_69	VSS_150
Y10	VSS_70	VSS_151
Y11	VSS_71	VSS_152
Y13	VSS_72	VSS_153
Y14	VSS_73	VSS_154
Y37	VSS_74	VSS_155
Y38	VSS_75	VSS_156
Y7	VSS_76	VSS_157
Y8	VSS_77	VSS_158
Y9	VSS_78	VSS_159
AK29	VSS_79	VSS_160
AK30	VSS_80	VSS_161
	VSS_81	VSS_162

CFL-H\_BGA1440  
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CFL-H		
UH1G		
AW5	VSS_163	VSS_244
AY12	VSS_164	VSS_245
AY33	VSS_165	VSS_246
AY34	VSS_166	VSS_247
B8	VSS_167	VSS_248
BA10	VSS_168	VSS_249
BA11	VSS_169	VSS_250
BA12	VSS_170	VSS_251
BA37	VSS_171	VSS_252
BA38	VSS_172	VSS_253
BA6	VSS_173	VSS_254
BA7	VSS_174	VSS_255
BA8	VSS_175	VSS_256
BA9	VSS_176	VSS_257
BB1	VSS_177	VSS_258
BB2	VSS_178	VSS_259
BB29	VSS_179	VSS_260
BB3	VSS_180	VSS_261
BB30	VSS_181	VSS_262
BB5	VSS_182	VSS_263
BB4	VSS_183	VSS_264
BB5	VSS_184	VSS_265
BC12	VSS_185	VSS_266
BC13	VSS_186	VSS_267
BC14	VSS_187	VSS_268
BC33	VSS_188	VSS_269
BC34	VSS_189	VSS_270
BC6	VSS_190	VSS_271
BD10	VSS_191	VSS_272
BD11	VSS_192	VSS_273
BD12	VSS_193	VSS_274
BD37	VSS_194	VSS_275
BD6	VSS_195	VSS_276
BD7	VSS_196	VSS_277
BD8	VSS_197	VSS_278
BD9	VSS_198	VSS_279
BE1	VSS_199	VSS_280
BE2	VSS_200	VSS_281
BE29	VSS_201	VSS_282
BE3	VSS_202	VSS_283
BE30	VSS_203	VSS_284
BE4	VSS_204	VSS_285
BE5	VSS_205	VSS_286
BE6	VSS_206	VSS_287
BF12	VSS_207	VSS_288
BF33	VSS_208	VSS_289
BF34	VSS_209	VSS_290
BF6	VSS_210	VSS_291
BG12	VSS_211	VSS_292
BG13	VSS_212	VSS_293
BG14	VSS_213	VSS_294
BG37	VSS_214	VSS_295
BG38	VSS_215	VSS_296
BG6	VSS_216	VSS_297
BH1	VSS_217	VSS_298
BH10	VSS_218	VSS_299
BH11	VSS_219	VSS_300
BH12	VSS_220	VSS_301
BH14	VSS_221	VSS_302
BH2	VSS_222	VSS_303
BH3	VSS_223	VSS_304
BH4	VSS_224	VSS_305
BH5	VSS_225	VSS_306
BH6	VSS_226	VSS_307
BH7	VSS_227	VSS_308
BH8	VSS_228	VSS_309
BH9	VSS_229	VSS_310
I2	VSS_230	VSS_311
I3	VSS_231	VSS_312
I33	VSS_232	VSS_313
I34	VSS_233	VSS_314
I4	VSS_234	VSS_315
I5	VSS_235	VSS_316
I7	VSS_236	VSS_317
I8	VSS_237	VSS_318
I9	VSS_238	VSS_319
I37	VSS_239	VSS_320
I38	VSS_240	VSS_321
I39	VSS_241	VSS_322
I42	VSS_242	VSS_323
I43	VSS_243	VSS_324

CFL-H\_BGA1440  
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CFL-H		
UH1H		
BN4	VSS_325	VSS_409
BN7	VSS_326	VSS_410
BP12	VSS_327	VSS_411
BP14	VSS_328	VSS_412
BP16	VSS_329	VSS_413
BP21	VSS_330	VSS_414
BP24	VSS_331	VSS_415
BP25	VSS_332	VSS_416
BP26	VSS_333	VSS_417
BP29	VSS_334	VSS_418
BP33	VSS_335	VSS_419
BP34	VSS_336	VSS_420
BP7	VSS_337	VSS_421
BR12	VSS_338	VSS_422
BR14	VSS_339	VSS_423
BR18	VSS_340	VSS_424
BR21	VSS_341	VSS_425
BR24	VSS_342	VSS_426
BR25	VSS_343	VSS_427
BR26	VSS_344	VSS_428
BR29	VSS_345	VSS_429
BR4	VSS_346	VSS_430
BR36	VSS_347	VSS_431
BR7	VSS_348	VSS_432
BT12	VSS_349	VSS_433
BT14	VSS_350	VSS_434
BT18	VSS_351	VSS_435
BT21	VSS_352	VSS_436
BT24	VSS_353	VSS_437
BT26	VSS_354	VSS_438
BT29	VSS_355	VSS_439
BT32	VSS_356	VSS_440
BT5	VSS_357	VSS_441
C11	VSS_358	VSS_442
C13	VSS_359	VSS_443
C15	VSS_360	VSS_444
C17	VSS_361	VSS_445
C19	VSS_362	VSS_446
C21	VSS_363	VSS_447
C23	VSS_364	VSS_448
C25	VSS_365	VSS_449
C27	VSS_366	VSS_450
C29	VSS_367	VSS_451
C31	VSS_368	VSS_452
C37	VSS_369	VSS_453
C5	VSS_370	VSS_454
C8	VSS_371	VSS_455
C9	VSS_372	VSS_456
D10	VSS_373	VSS_457
D12	VSS_374	VSS_458
D14	VSS_375	VSS_459
D16	VSS_376	VSS_460
D18	VSS_377	VSS_461
D20	VSS_378	VSS_462
D22	VSS_379	VSS_463
D24	VSS_380	VSS_464
D26	VSS_381	VSS_465
D28	VSS_382	VSS_466
D3	VSS_383	VSS_467
D30	VSS_384	VSS_468
D33	VSS_385	VSS_469
D6	VSS_386	VSS_470
D9	VSS_387	VSS_471
E34	VSS_388	VSS_472
E35	VSS_389	VSS_473
E38	VSS_390	VSS_474
E4	VSS_391	VSS_475
E9	VSS_392	VSS_476
N3	VSS_393	VSS_477
N33	VSS_394	VSS_478
N34	VSS_395	VSS_479
N4	VSS_396	VSS_480
N5	VSS_397	VSS_481
N6	VSS_398	VSS_482
N7	VSS_399	VSS_483
N8	VSS_400	VSS_484
N9	VSS_401	VSS_485
P12	VSS_402	VSS_486
P37	VSS_403	VSS_487
M14	VSS_404	VSS_488
M6	VSS_405	VSS_489
N1	VSS_406	VSS_490
F11	VSS_407	VSS_491
F13	VSS_408	VSS_492

CFL-H\_BGA1440  
@

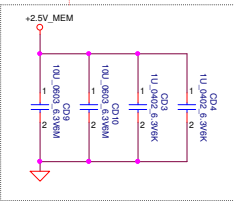
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F17	VSS_411	VSS_412
F19	VSS_413	VSS_414
F2	VSS_415	VSS_416
F21	VSS_417	VSS_418
F23	VSS_419	VSS_420
F25	VSS_421	VSS_422
F27	VSS_423	VSS_424
F29	VSS_425	VSS_426
F3	VSS_427	VSS_428
F31	VSS_429	VSS_430
F36	VSS_431	VSS_432
F4	VSS_433	VSS_434
F5	VSS_435	VSS_436
F8	VSS_437	VSS_438
F9	VSS_439	VSS_440
G10	VSS_441	VSS_442
G12	VSS_443	VSS_444
G14	VSS_445	VSS_446
G16	VSS_447	VSS_448
G18	VSS_449	VSS_450
G20	VSS_451	VSS_452
G22	VSS_453	VSS_454
G23	VSS_455	VSS_456
G24	VSS_457	VSS_458
G26	VSS_459	VSS_460
G28	VSS_461	VSS_462
G4	VSS_463	VSS_464
G5	VSS_465	VSS_466
G6	VSS_467	VSS_468
G8	VSS_469	VSS_470
G9	VSS_471	VSS_472
H11	VSS_473	VSS_474
H12	VSS_475	VSS_476
H18	VSS_477	VSS_478
H22	VSS_479	VSS_480
H25	VSS_481	VSS_482
H32	VSS_483	VSS_484
H35	VSS_485	VSS_486
J10	VSS_487	VSS_488
J18	VSS_489	VSS_490
J22	VSS_491	VSS_492
J25	VSS_493	VSS_494
J32	VSS_495	VSS_496
J33	VSS_497	VSS_498
J36	VSS_499	VSS_500
J4	VSS_501	VSS_502
K1	VSS_503	VSS_504
K10	VSS_505	VSS_506
K11	VSS_507	VSS_508
K2	VSS_509	VSS_510
K3	VSS_511	VSS_512
K38	VSS_513	VSS_514
K4	VSS_515	VSS_516
K5	VSS_517	VSS_518
K7	VSS_519	VSS_520
K8	VSS_521	VSS_522
K9	VSS_523	VSS_524
L29	VSS_525	VSS_526
L30	VSS_527	VSS_528
L33	VSS_529	VSS_530
L34	VSS_531	VSS_532
M12	VSS_533	VSS_534
M13	VSS_535	VSS_536
N10	VSS_537	VSS_538
N11	VSS_539	VSS_540
N12	VSS_541	VSS_542
N2	VSS_543	VSS_544
BT8	VSS_545	VSS_546
BR9	VSS_547	VSS_548
A3	VSS_549	VSS_550
A34	VSS_551	VSS_552
A4	VSS_553	VSS_554
B3	VSS_555	VSS_556
B37	VSS_557	VSS_558
BR38	VSS_559	VSS_560
BT3	VSS_561	VSS_562
BT35	VSS_563	VSS_564
BT36	VSS_565	VSS_566
BT4	VSS_567	VSS_568
C2	VSS_569	VSS_570
D38	VSS_571	VSS_572

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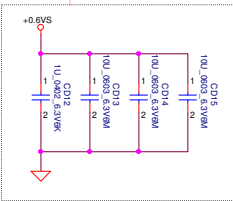
Compal Electronics, Inc.

P13-CPU(7/7) VSS

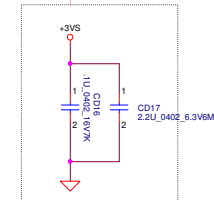
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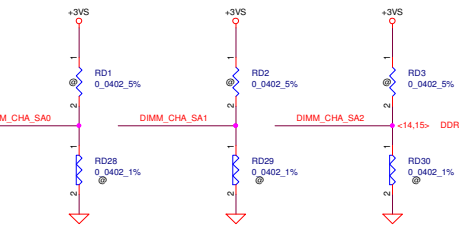
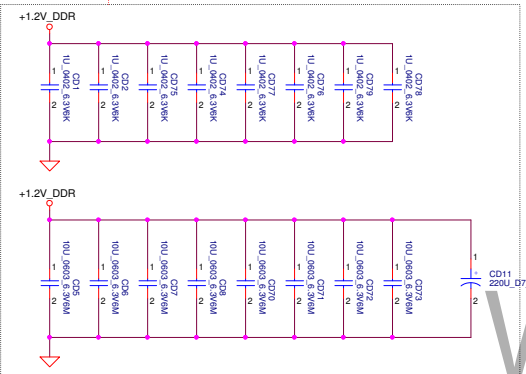
Layout Note:  
Place near JDIMM1.258



Layout Note:  
Place near JDIMM1.255



Layout Note:  
Place near JDIMM1



VREF traces should be at least 20 mils wide with 20 mils spacing to other signals

CPU Side

+V\_DDR\_REFA\_R

20mil

RH484 1

CH101 0.022u 0.402 25V7K

RH211 24.9 0.402 1%

DIMM Side

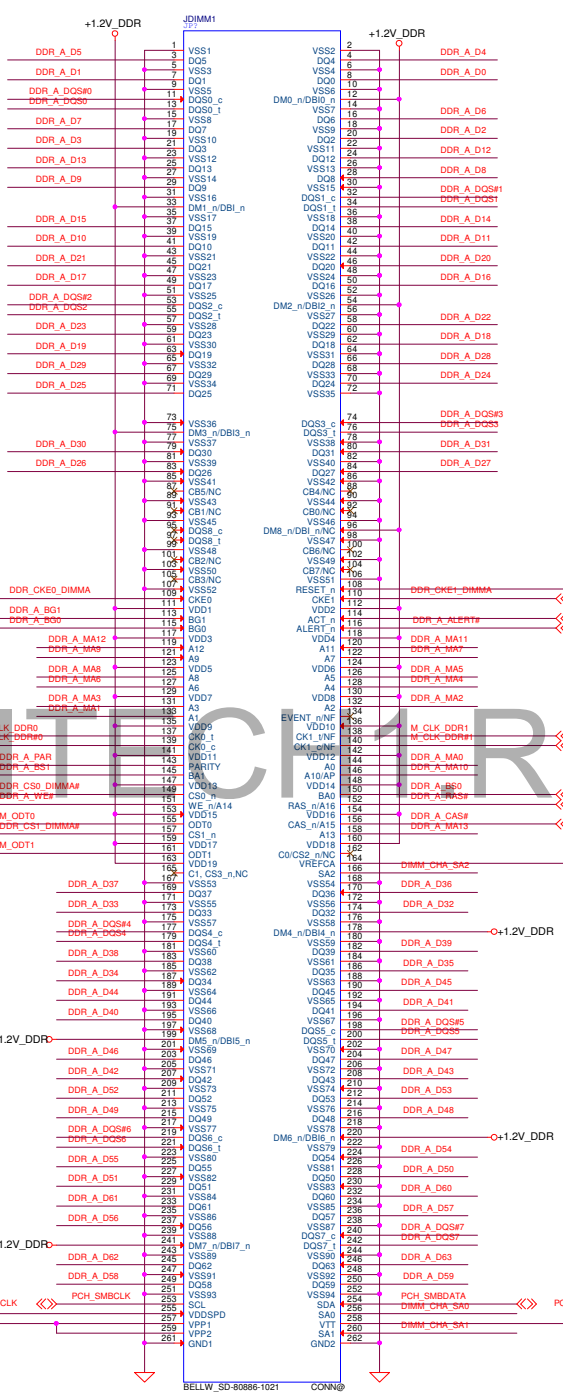
+V\_DDR\_REFA

20mil

RH206 1K 0.402 1%

RH209 1K 0.402 1%

<B> DDR\_A\_D0..B31  
<B> DDR\_A\_MA0..13  
<B> DDR\_A\_DQS#0..7  
<B> DDR\_A\_DQS#0..7

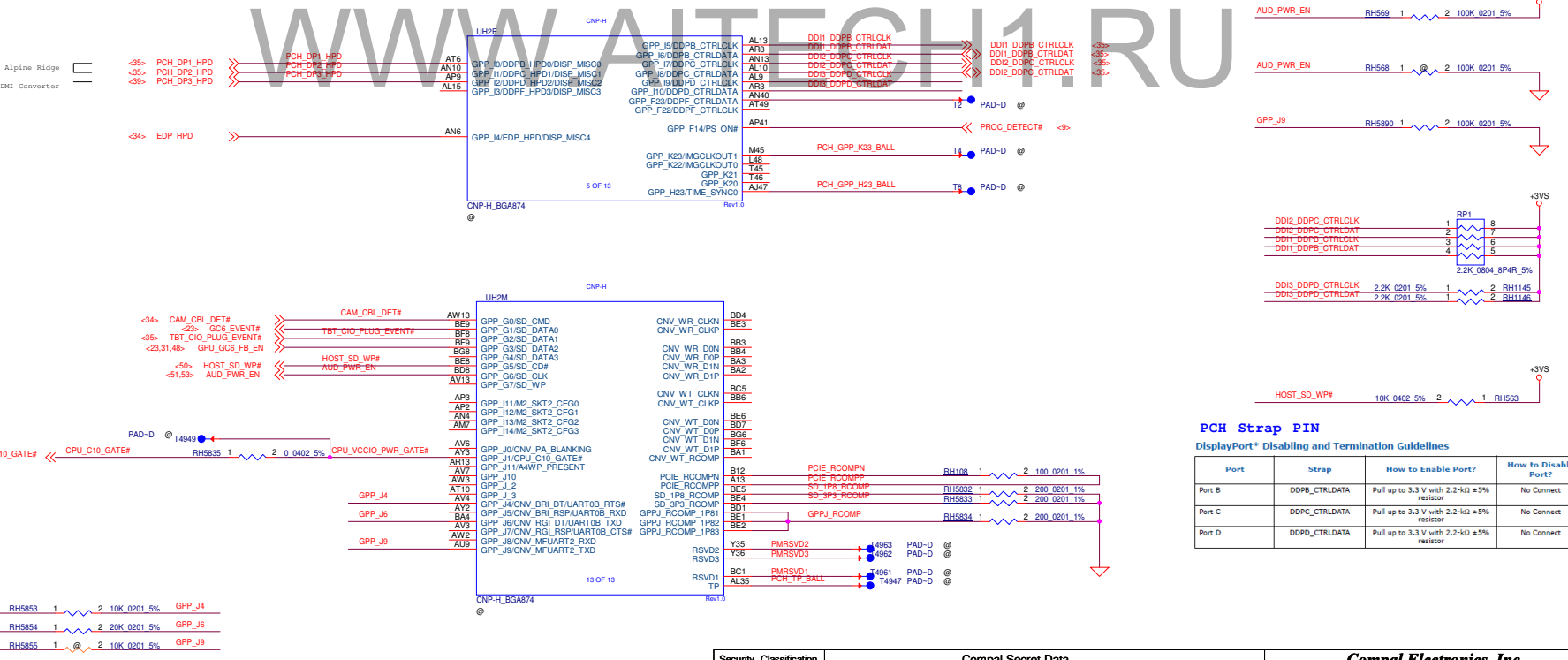
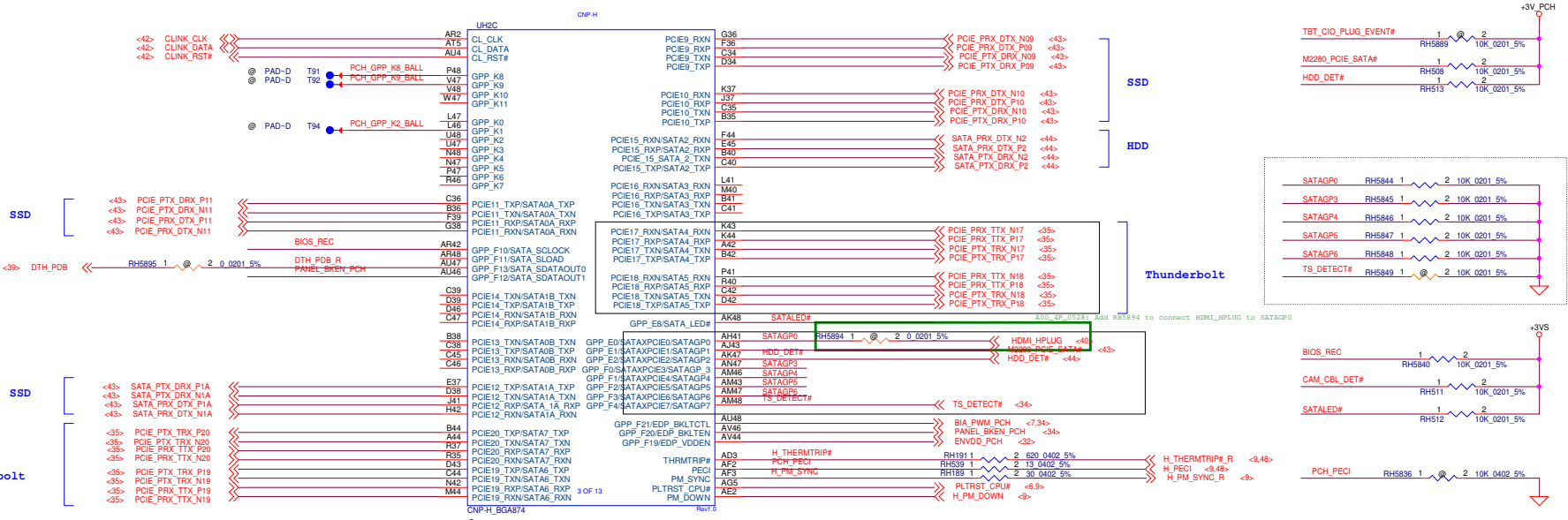


All VREF traces should have 10 mil trace width

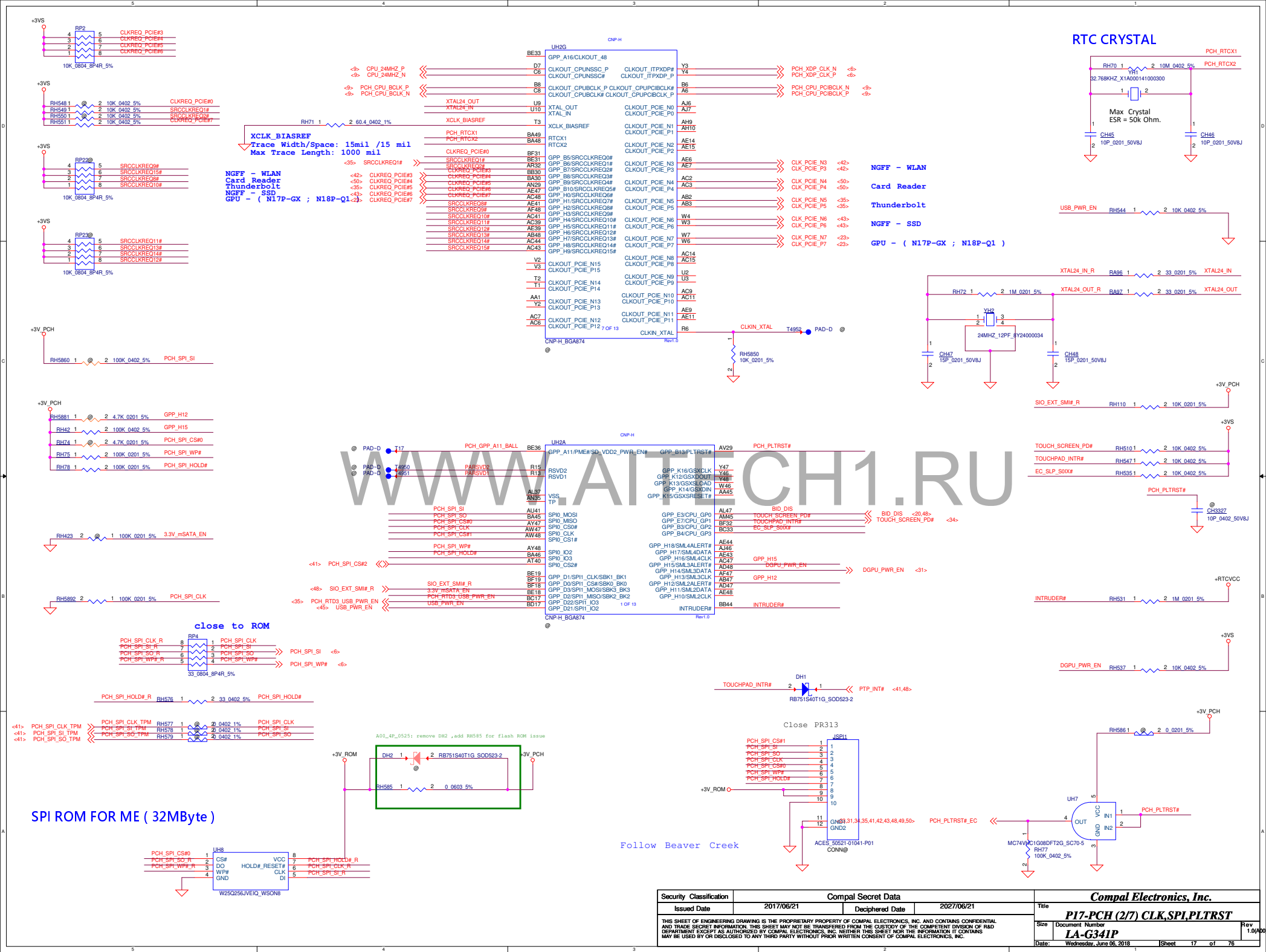
+V\_DDR\_REFA 20mil

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				Sheet	14 of 76

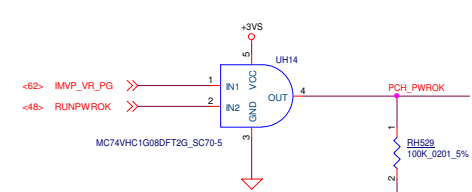
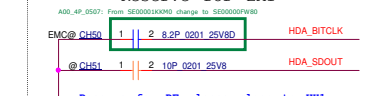
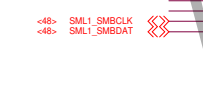
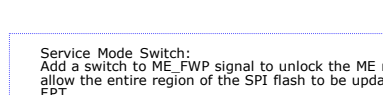
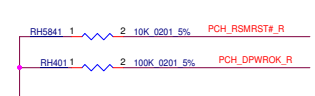




PCH Strap PIN			
DisplayPort* Disabling and Termination Guidelines			
Port	Strap	How to Enable Port?	How to Disable Port?
Port B	DD0B_CTRLCLK	Pull up to 3.3 V with 2.2-k $\Omega$ $\pm$ 5% resistor	No Connect
Port C	DD0C_CTRLCLK	Pull up to 3.3 V with 2.2-k $\Omega$ $\pm$ 5% resistor	No Connect
Port D	DD0D_CTRLCLK	Pull up to 3.3 V with 2.2-k $\Omega$ $\pm$ 5% resistor	No Connect



1=Disable ME Protect (ME can be updated)  
0=Enable ME Protect (ME cannot be updated)

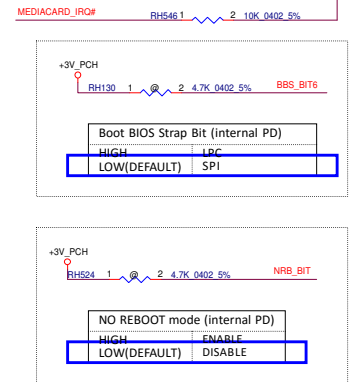


Disable ME Protect (ME can be updated) ----> Pin1 & Pin2 short  
Enable ME Protect (ME cannot be updated)-->Pin3 & Pin2 short(Default position)

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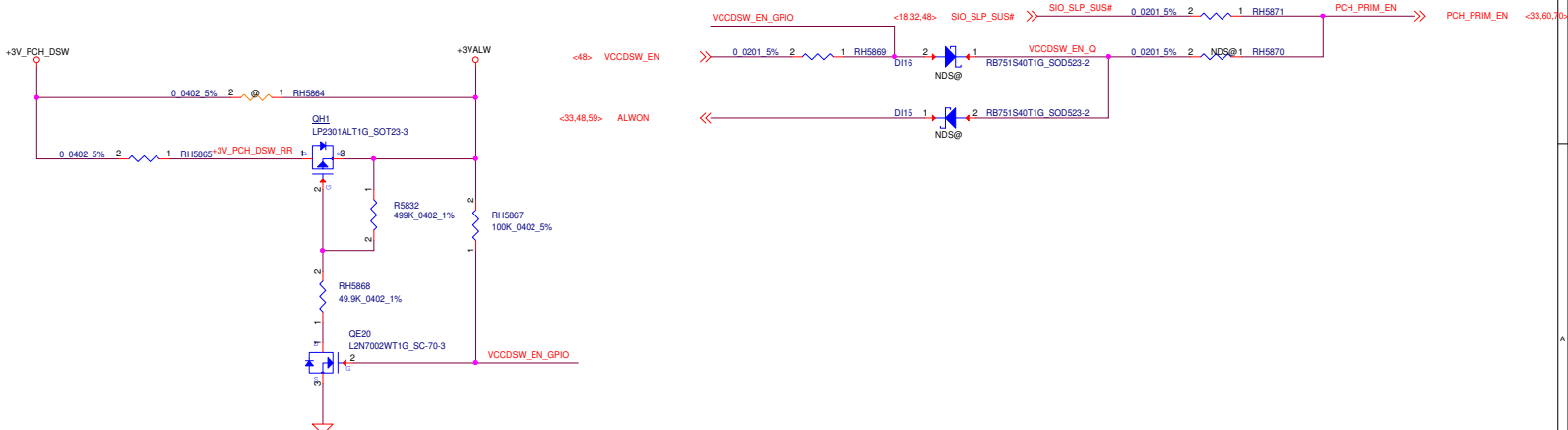
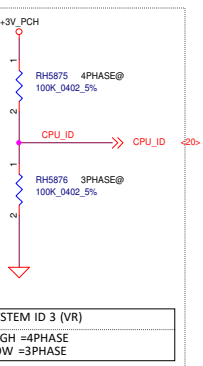




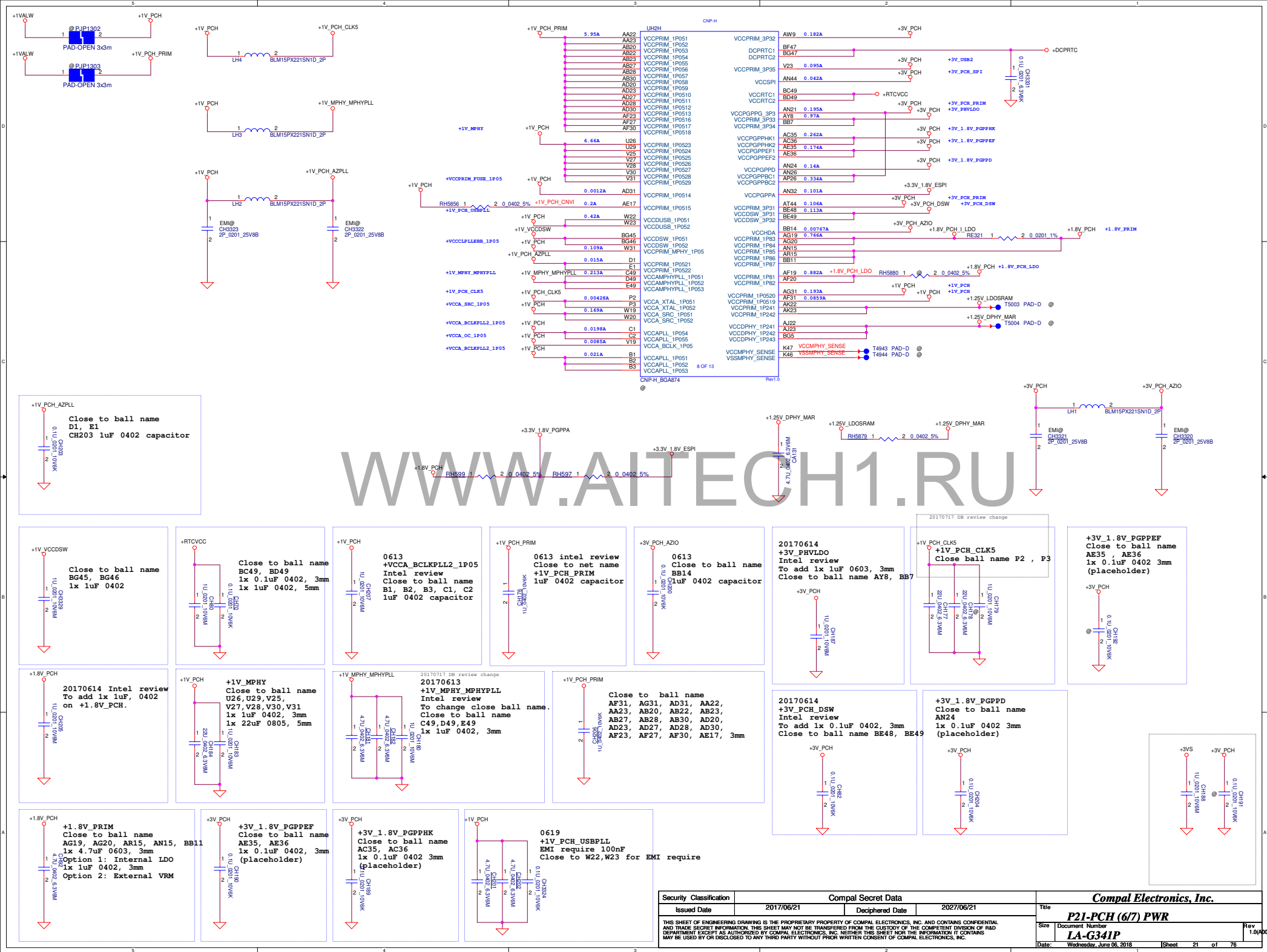


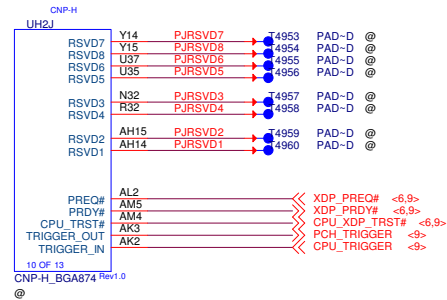
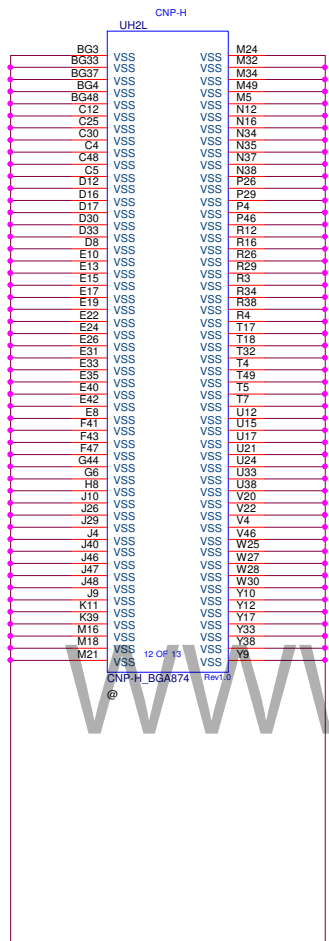
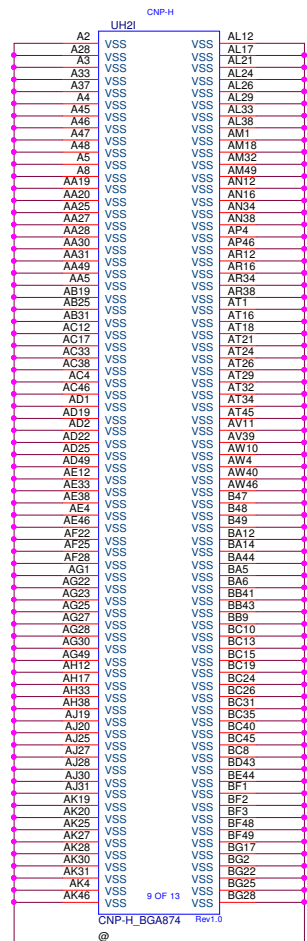
Three schematic diagrams illustrating the connection of the BID\_DIS pin to different components:

- Left Diagram:** The BID\_DIS pin is connected to a resistor RH564 (100K\_0402\_5%) and a capacitor RH565 (100K\_0402\_5%). The resistor is connected to the BID\_DIS pin, which is then connected to the GPU. The capacitor is connected to ground.
- Middle Diagram:** The BID\_DIS pin is connected to a resistor RH566 (100K\_0402\_5%) and a capacitor RH567 (100K\_0402\_5%). The resistor is connected to the BID\_DIS pin, which is then connected to the BC. The capacitor is connected to ground.
- Right Diagram:** The BID\_DIS pin is connected to a resistor RH567 (100K\_0201\_5%) and a capacitor RH568 (100K\_0201\_5%). The resistor is connected to the BID\_DIS pin, which is then connected to the GPU. The capacitor is connected to ground.

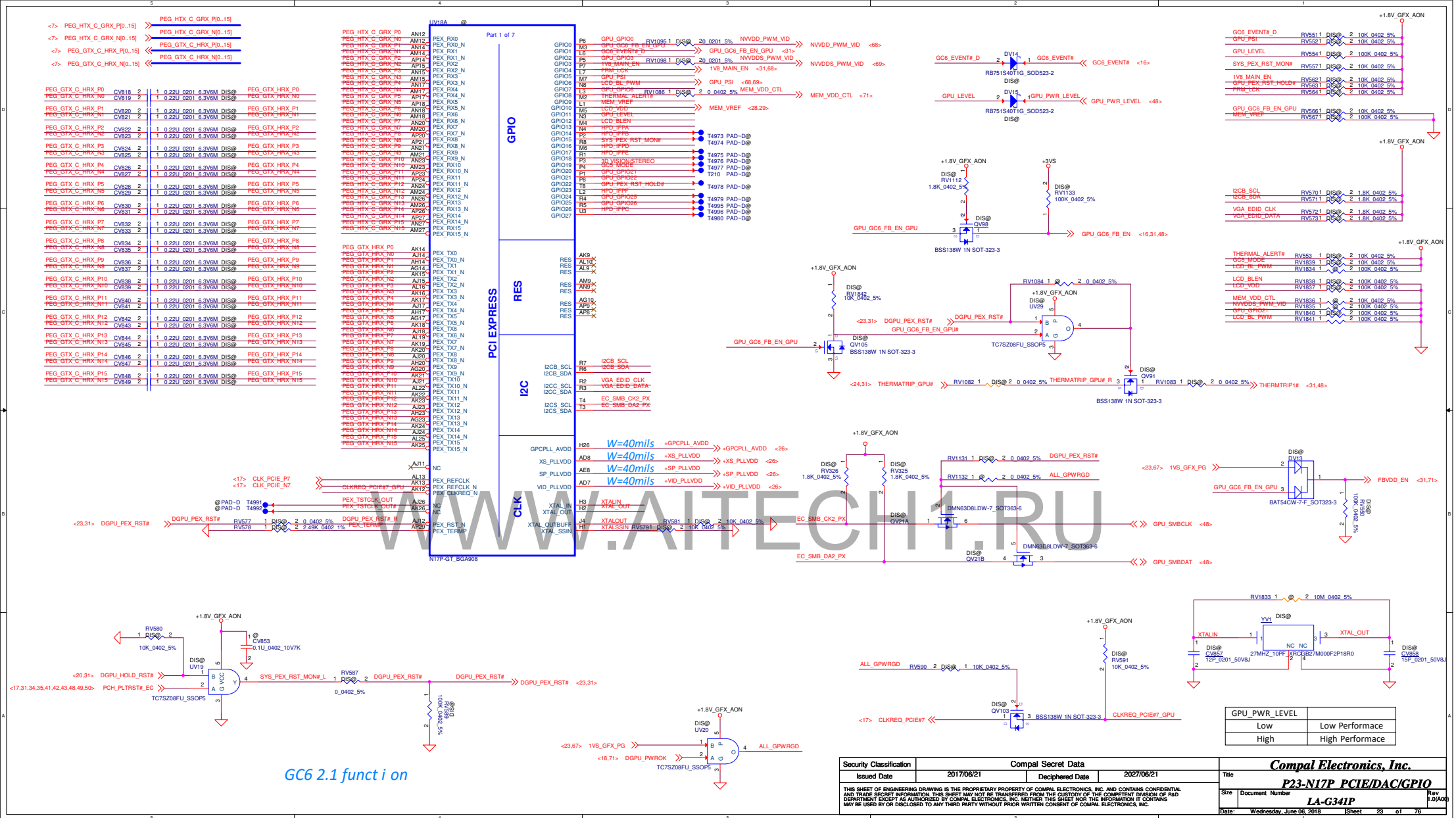




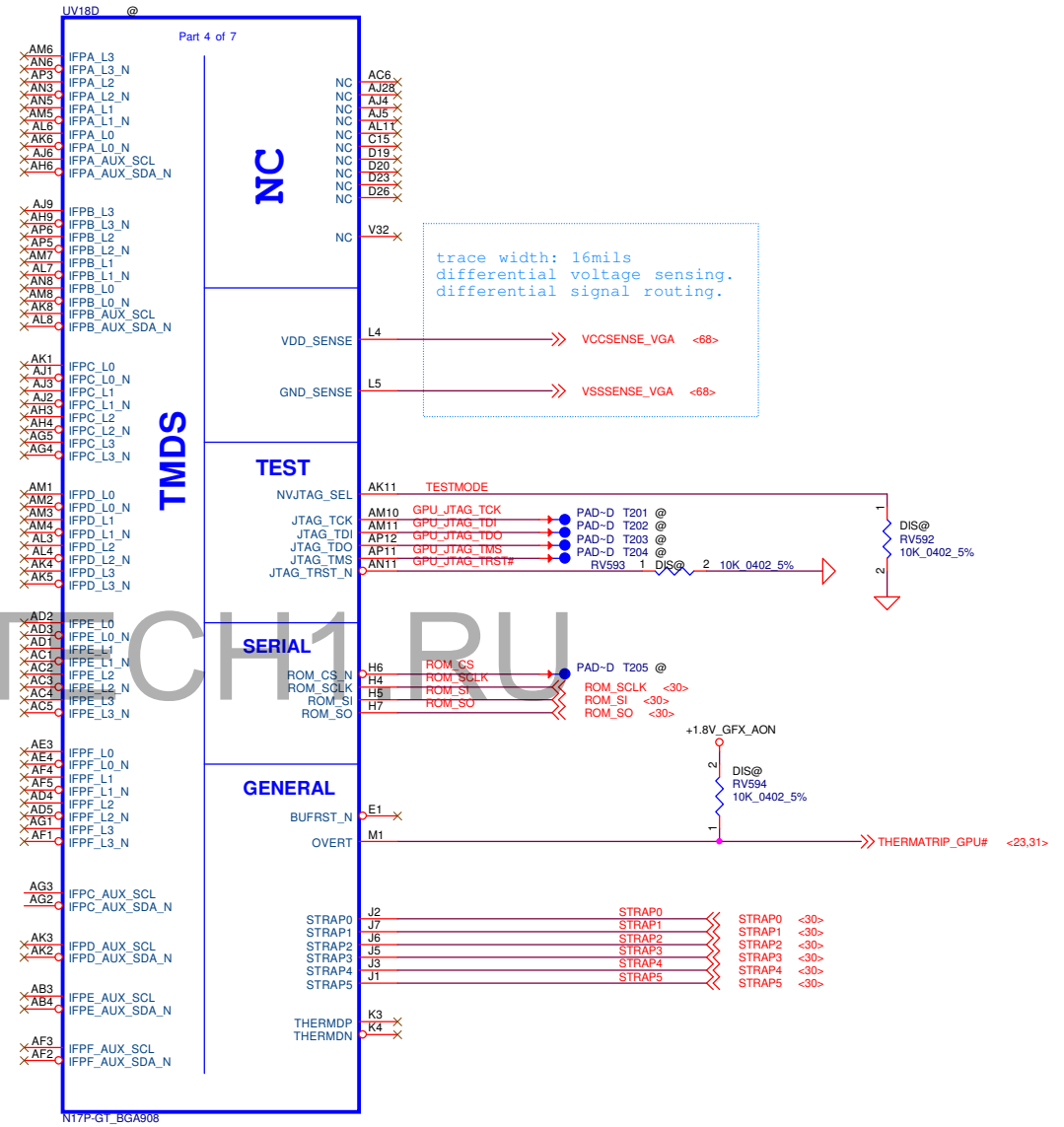




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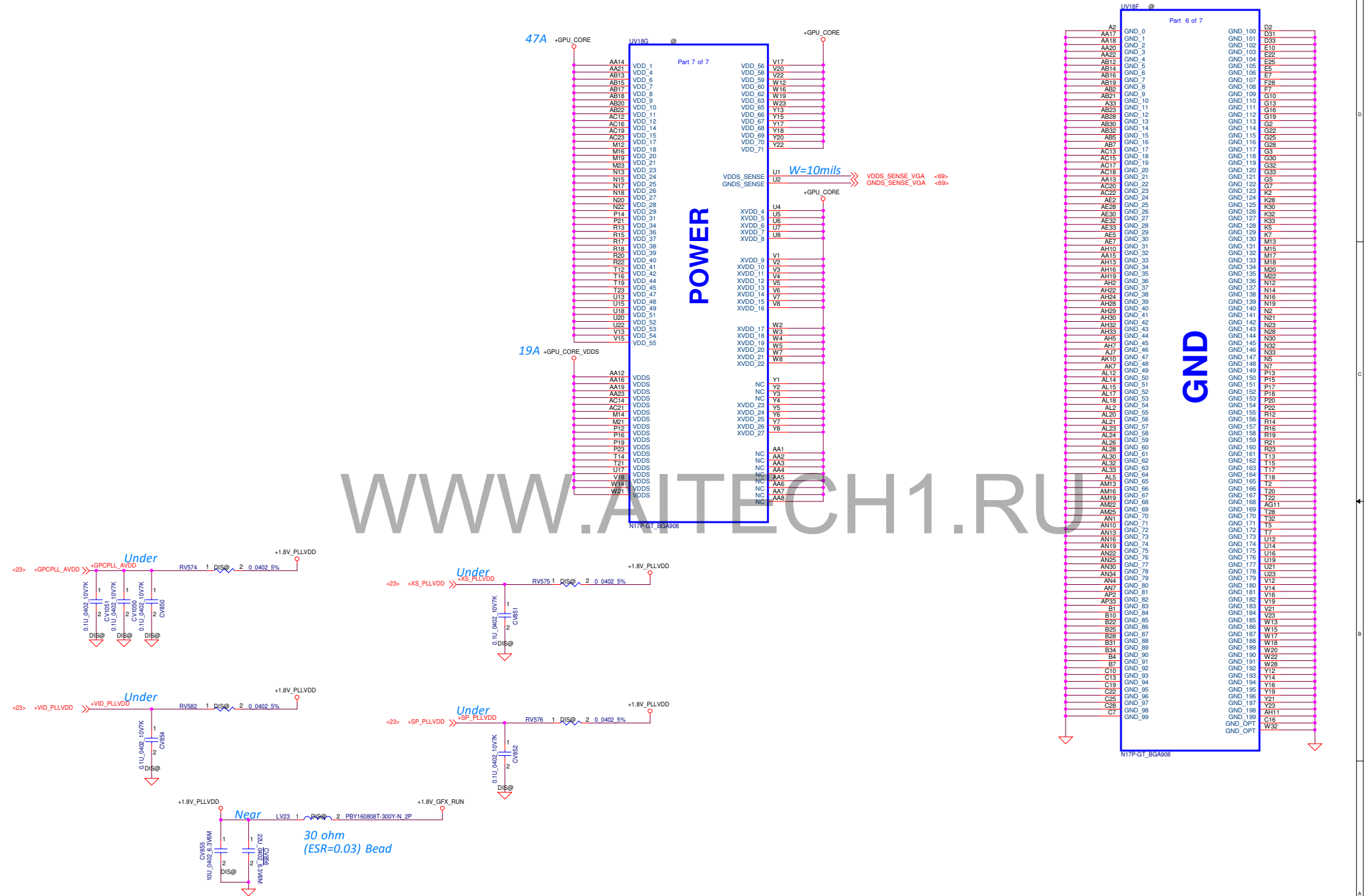


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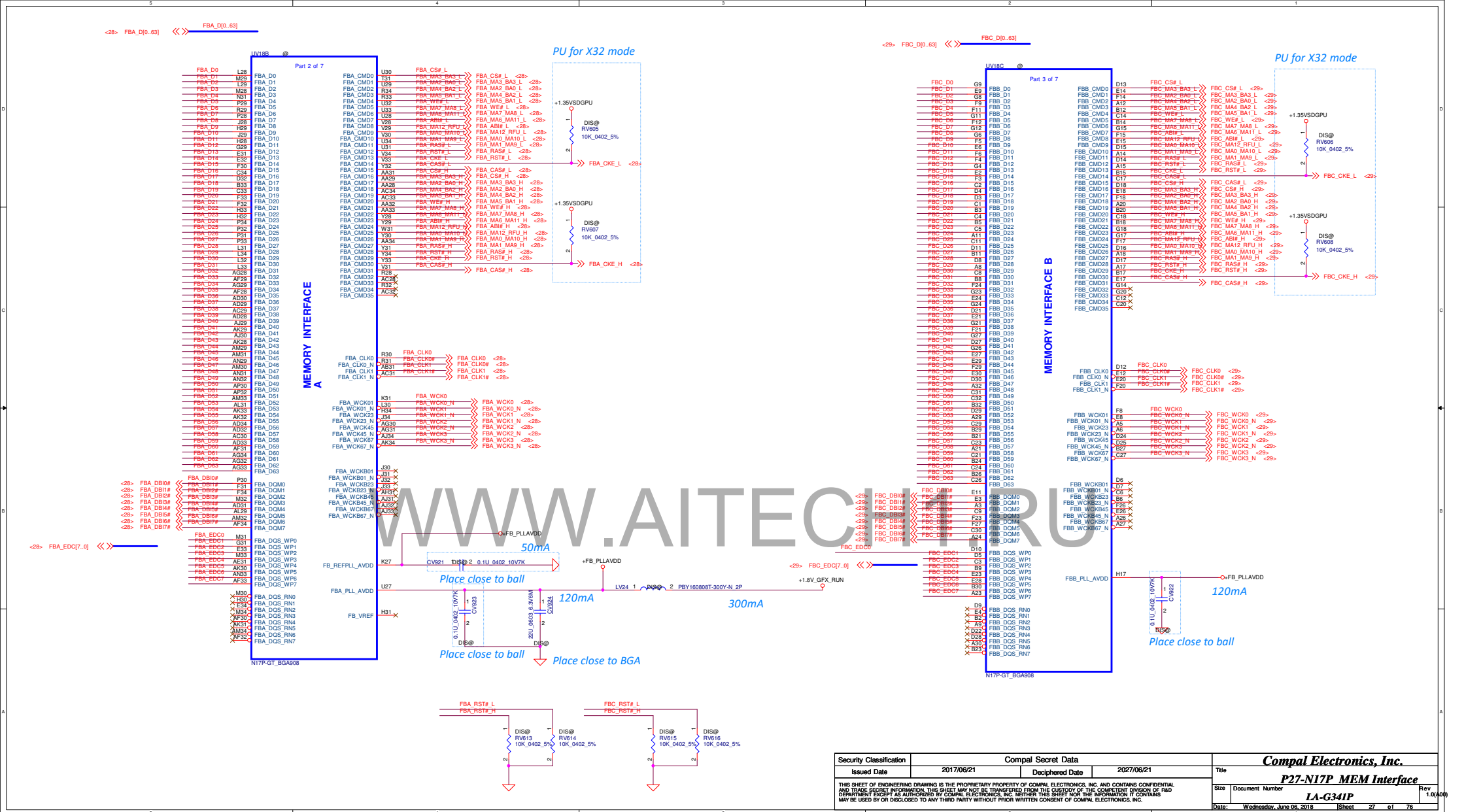


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						LA-G341P				1.0(Add)	
						Date:		Wednesday, June 06, 2018		Sheet 24 of 76	
						1		2		1	





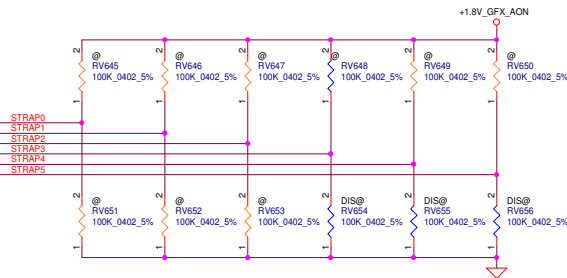
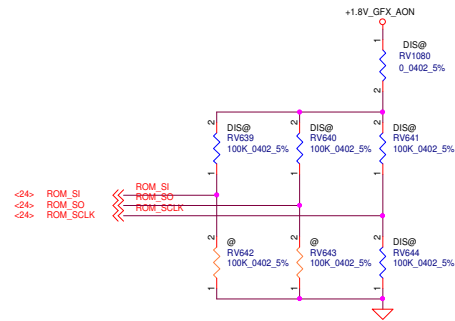












SMB_ALT_ADDR	State	DEVID_SEL	State	PCIE_CFG	State	VGA_DEVICE	State
Low	Single GPU	Low	Original Device	Low	Normal signal swing	Low	3D Device
High	Dual GPU	High	Re-brand Device ID	High	Reduce the signal amplitude	High	VGA Device

Table 5.5 SMB\_ALT\_ADDR, DEVID\_SEL, PCIE\_CFG, VGA\_DEVICE

Strap Pins <sup>Note 1</sup>			Functions Selected by This Strapping			
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	L	L	0	0	0	0

Table 5.2 RAMCFG

Strap Pins <sup>see Note</sup>			RAMCFG Setting Number	
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)	
L	L	L	0 (0x0000)	SAMSUNG
L	L	H	1 (0x0001)	MICRON
L	H	L	2 (0x0002)	HYNIX

Table 3. N17P-G0/-G1 GDDR5 Recommended Memories

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code	Qual Plan	Status
8 Gb	256Mx32	1.35V and 1.5V <sup>2</sup>	Samsung	K4G80325FB-HC28	B-die	0x0	7 Gbps	N/A	Full	Production ready
			Samsung	K4G80325FB-HC25	B-die	0x0	8 Gbps	N/A	N/A	Substitution allowed with waiver <sup>1</sup>
			Micron	MT51J256M32HF-70-A	A-die	0x1	7 Gbps	N/A	Full	Production ready
			Micron	MT51J256M32HF-80-A	A-die	0x1	8 Gbps	N/A	N/A	Substitution allowed with waiver <sup>1</sup>
			Hynix	H5GQ8H24MJR-R0C	M-die	0x2	7 Gbps	N/A	Full	Post production ready
			Hynix	H5GQ8H24MJR-R4C	M-die	0x2	8 Gbps	N/A	N/A	Substitution allowed with waiver <sup>1</sup>

Table 15-3. GB2B-64, GB4B-128 and GB3B-256 Multi-level Mode Strapping

Strap Pin Name	Logical Strapping Bit 3	Logical Strapping Bit 2	Logical Strapping Bit 1	Logical Strapping Bit 0
ROM_SCLK	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
ROM_SI	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	DEVID_SEL	PCIE_CFG	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	Keep foot print for pull-up to 3V3_AON and pull-down to GND. Stuff 49.9 kΩ pull-up.			
STRAP1	Keep foot print for pull-up to 3V3_AON and pull-down to GND.			
STRAP2	Do not stuff.			
STRAP3				
STRAP4				

Berlinetta MLK			
Straps	(N17P-Q1)	(N17P-G0)	
Net NAME	state	State	defind
ROM_SCLK	PD 5K	"M"	SOR_EXPOSED(LSB)
ROM_SI	Base on memory RVL	"H"	SOR_EXPOSED
ROM_SO	PD 5K	"H"	SOR_EXPOSED(MSB)
STRAP0	PU 49.9K		RAMCFG(LSB)
STRAP1	Do not stuff		RAMCFG
STRAP2	Do not stuff		RAMCFG(MSB)
STRAP3	Do not stuff	"L"	SMB_ALT_ADDR(0), DEVID_SEL(0)
STRAP4	Do not stuff	"L"	PCIE_CFG(0), VGA_DEVICE(0)
STRAP5	Unused	"L"	

Table 4. N17P-Q1 GDDR5 Recommended Memories

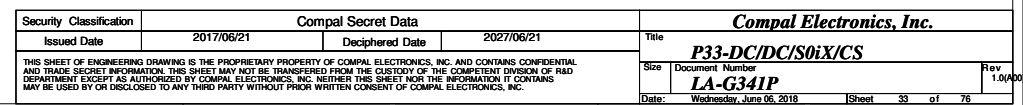
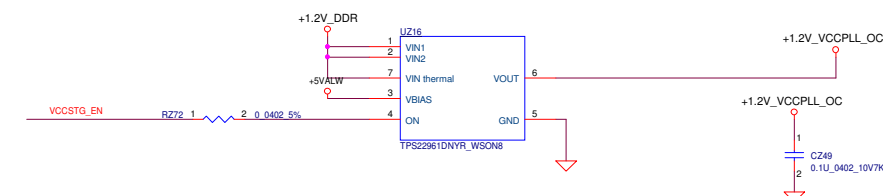
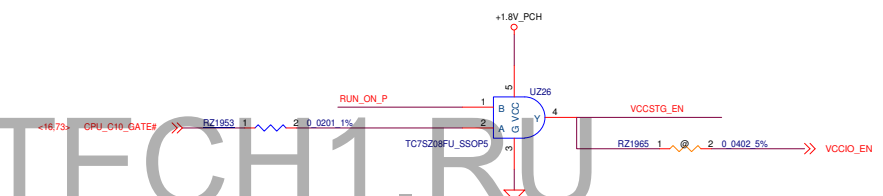
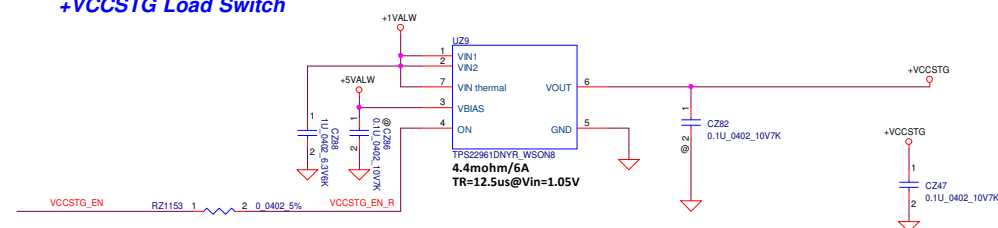
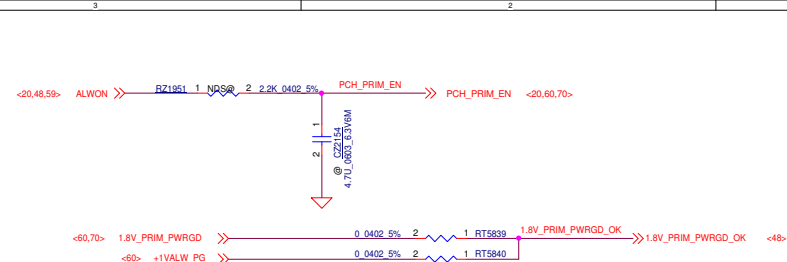
Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	256Mx32	1.35V	Samsung	K4G80325FB-HC03	B-die	0x8	6 Gbps	N/A	Full	Production candidate
			Micron	MT51J256M32HF-60:A	A-die	0x9	6 Gbps	N/A	Full	Production candidate

Notes:

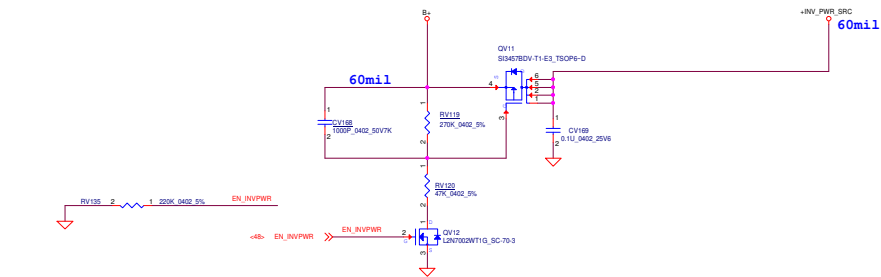
- For N17P-Q1, the maximum allowable memory case temperature is 85 °C.



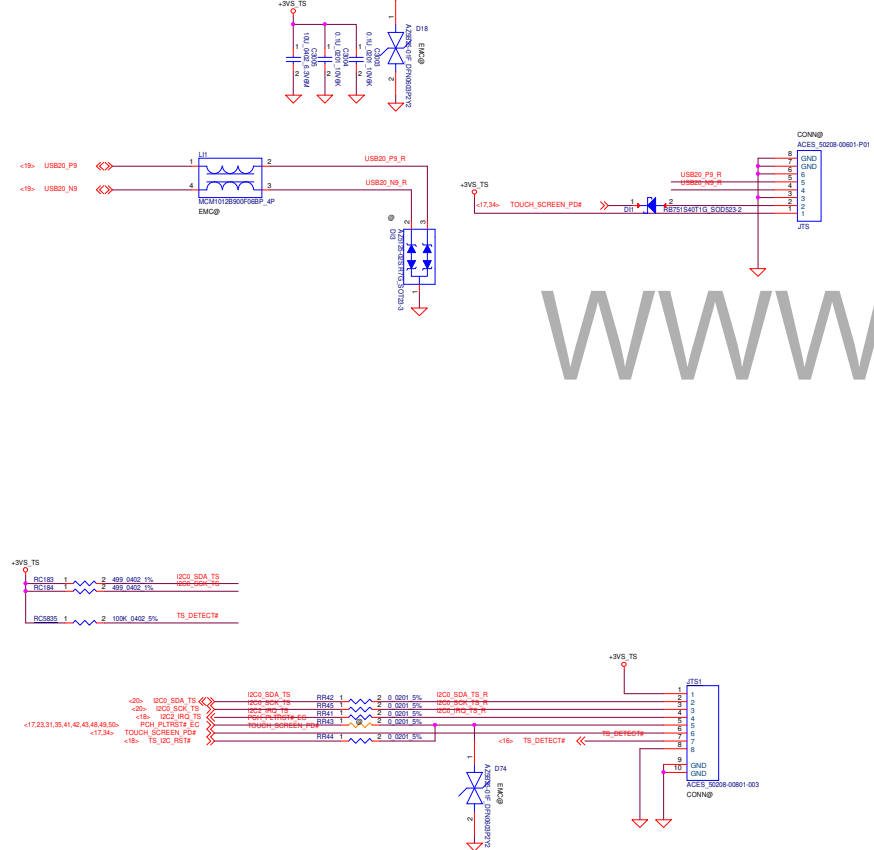




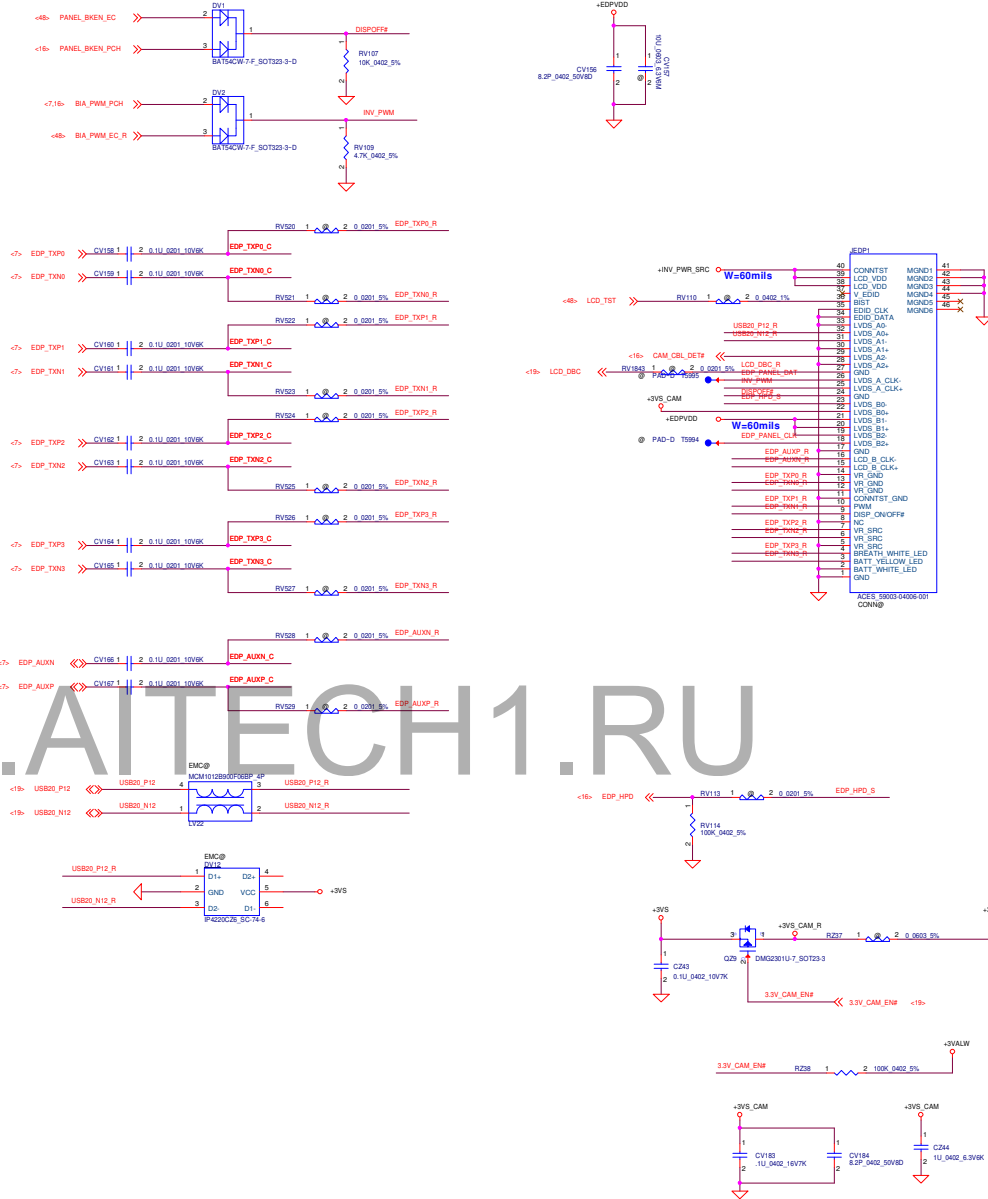
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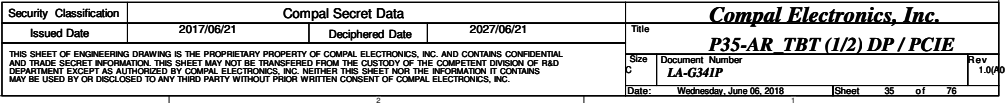


## Touch Screen Conn.

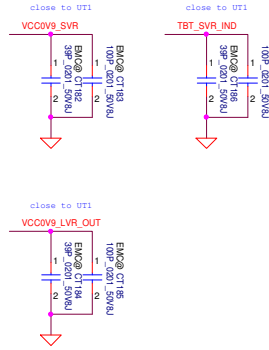
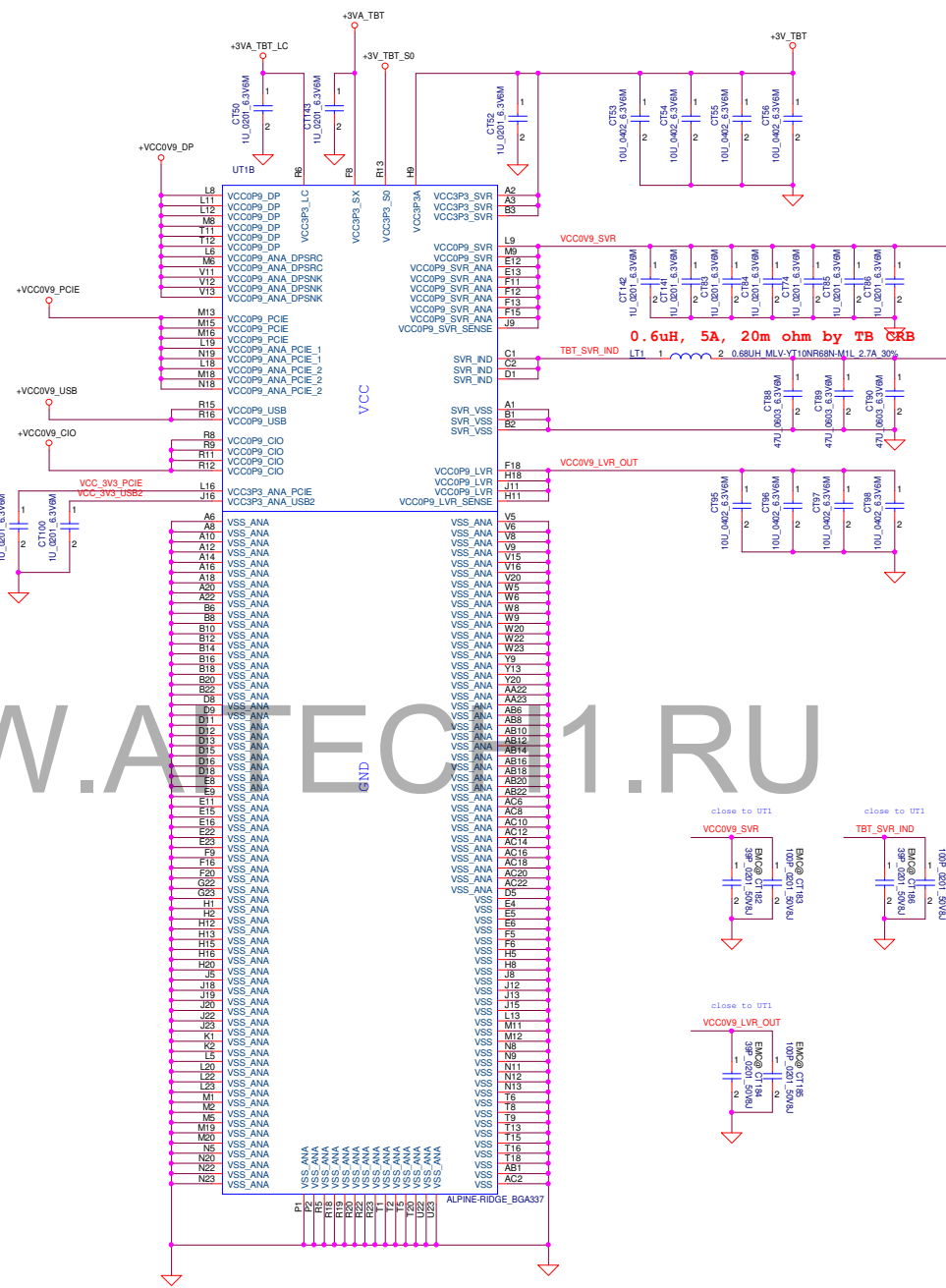
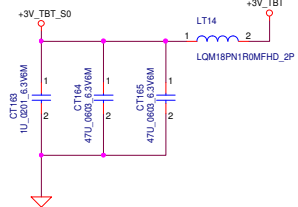
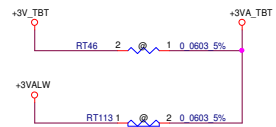


## eDP & CCD(RGB) Conn.

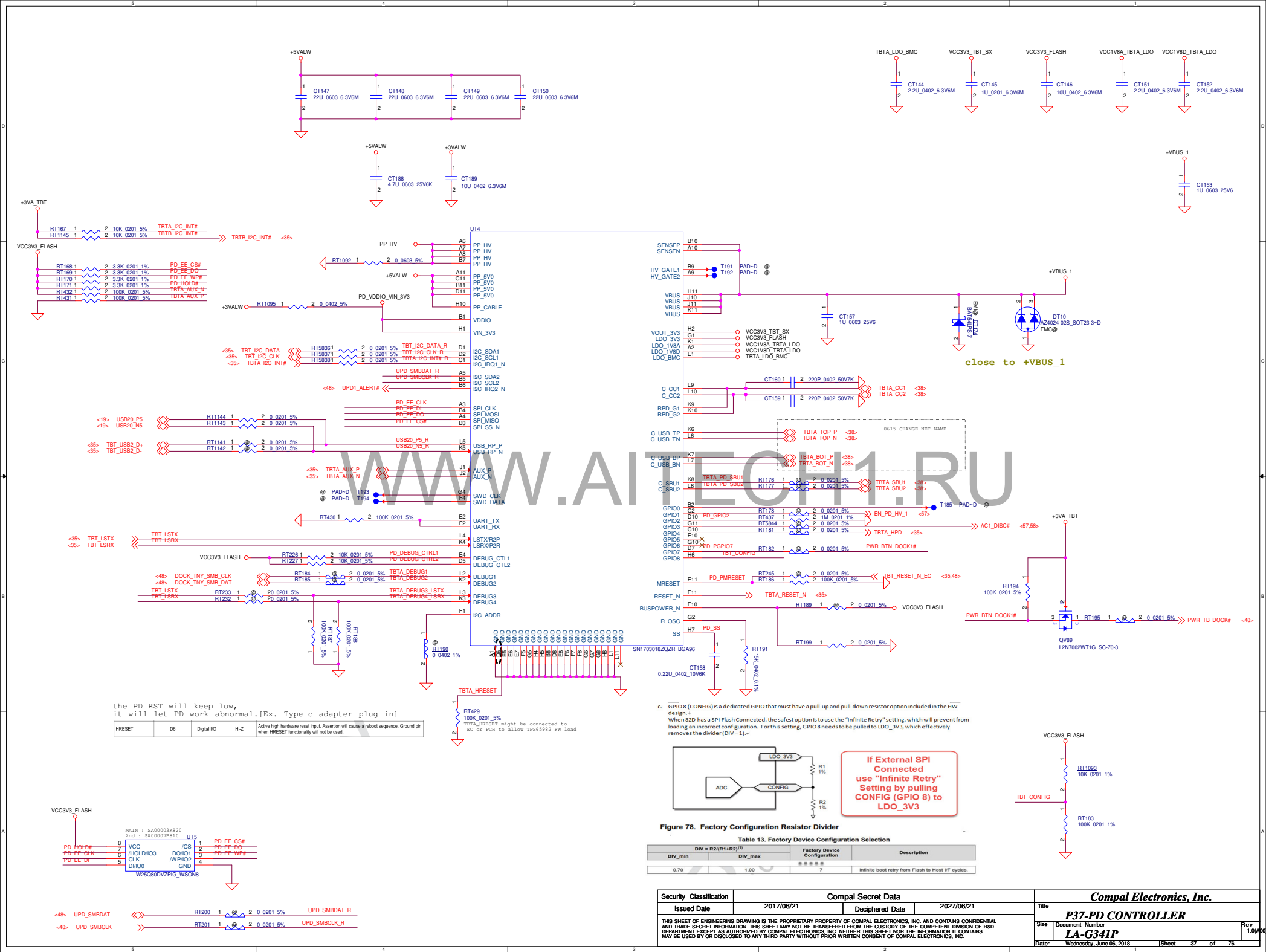


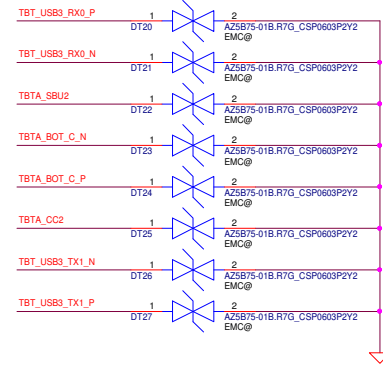
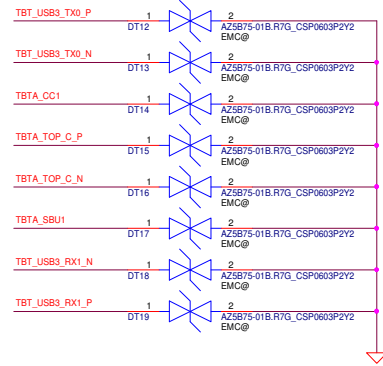
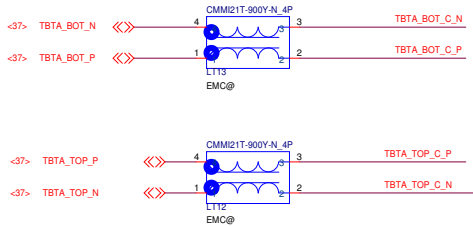




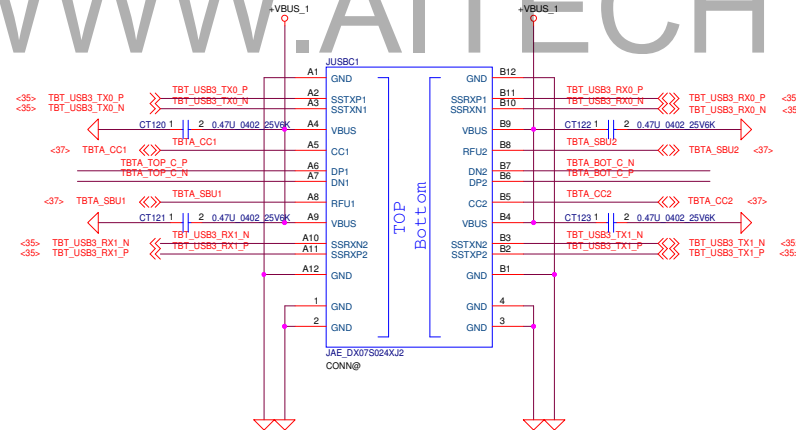
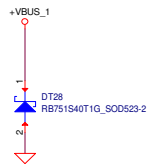




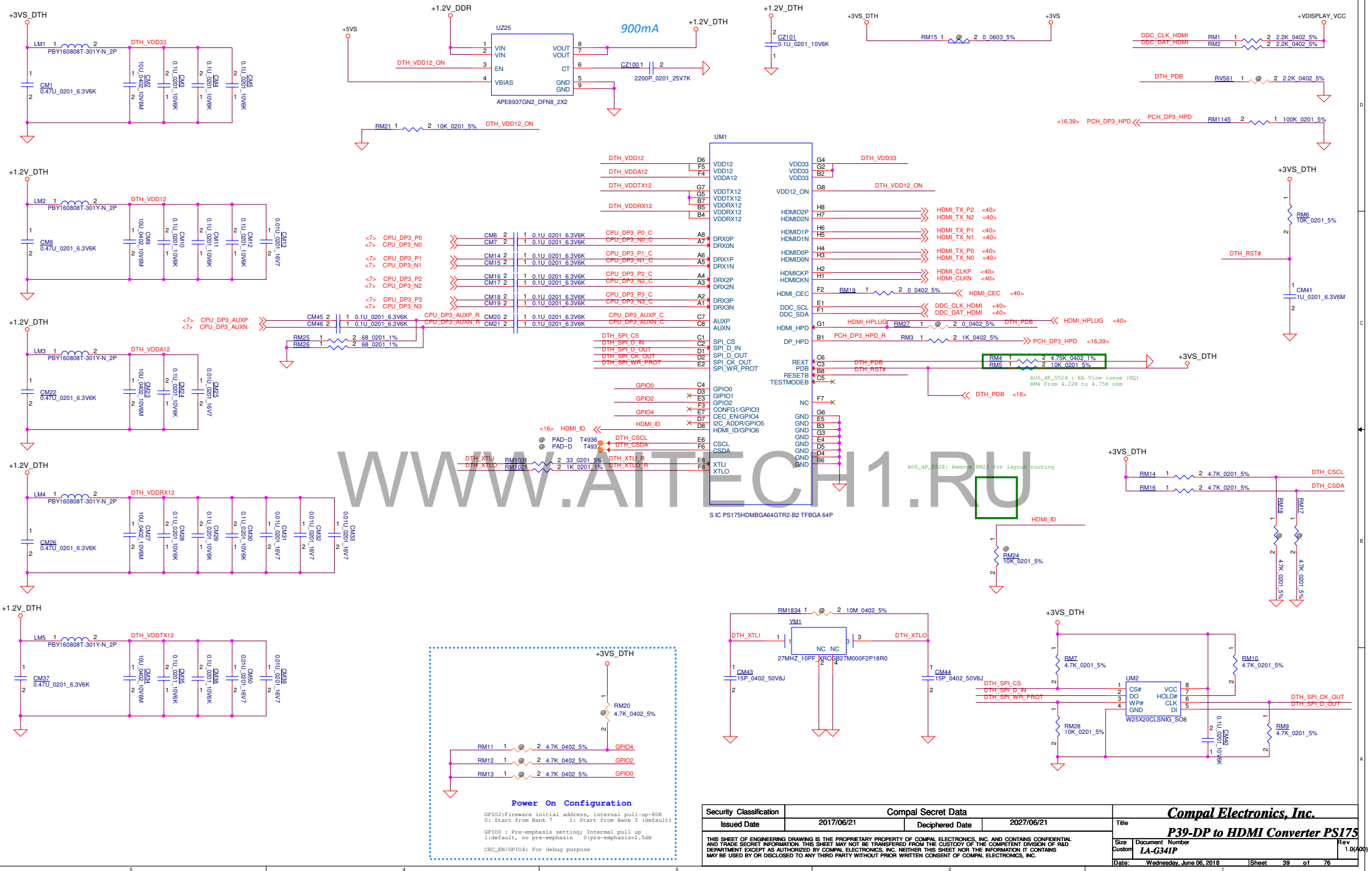




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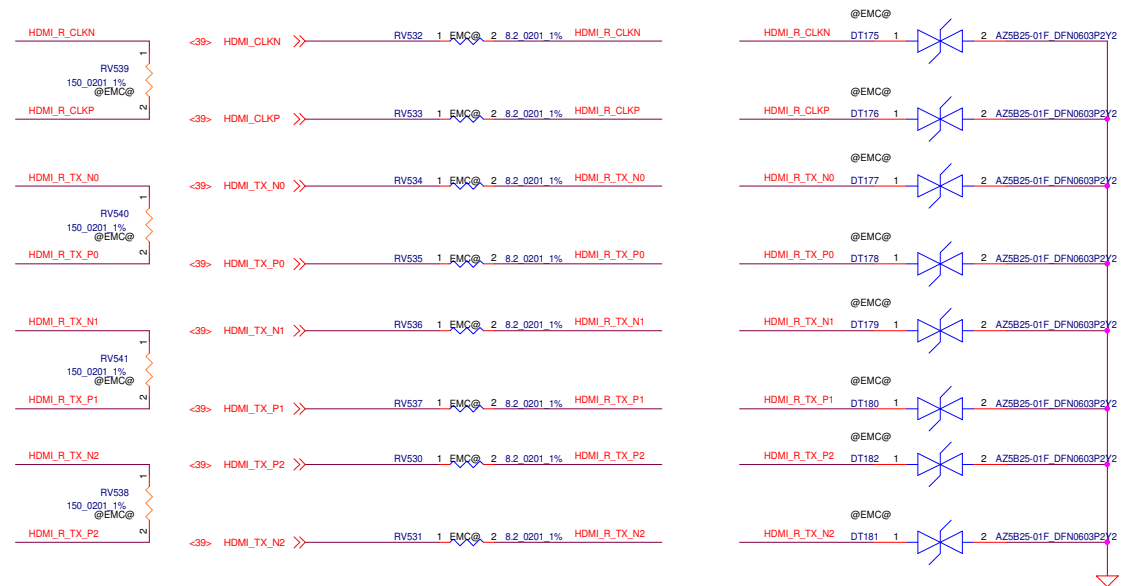


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				Rev	
				LA-G34IP	
				1.0/400	
				Date: Wednesday, June 06, 2018	
				Sheet 39 of 76	

HDMI change to CPU to PS185 to CONN

Place between ESD and CM-Choke

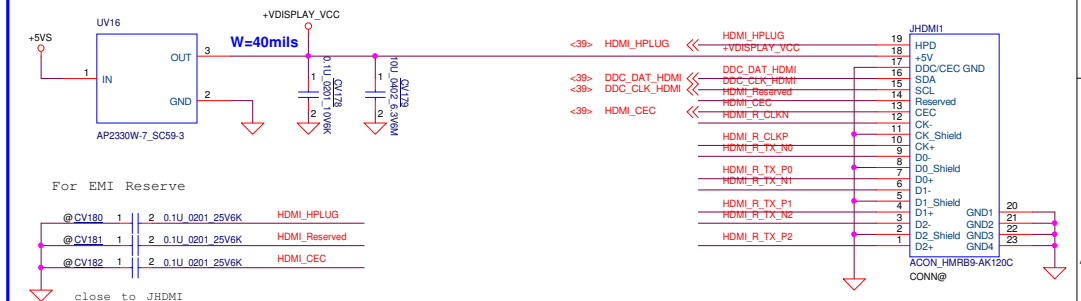
Place close to JHDMI1



WWW.AITECH1.RU

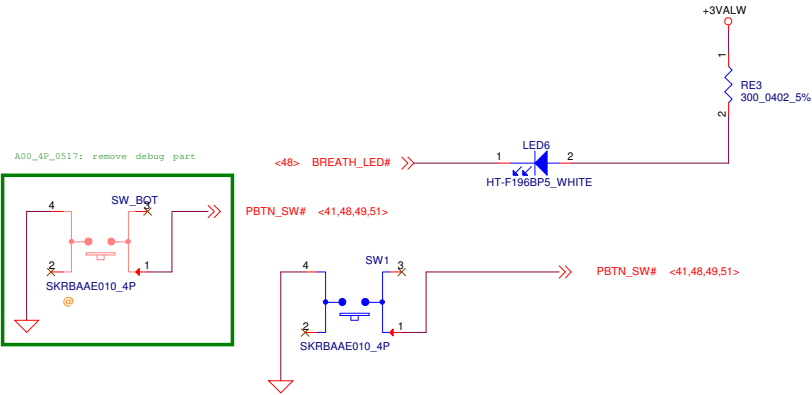
## HDMI DDC

## HDMI conn

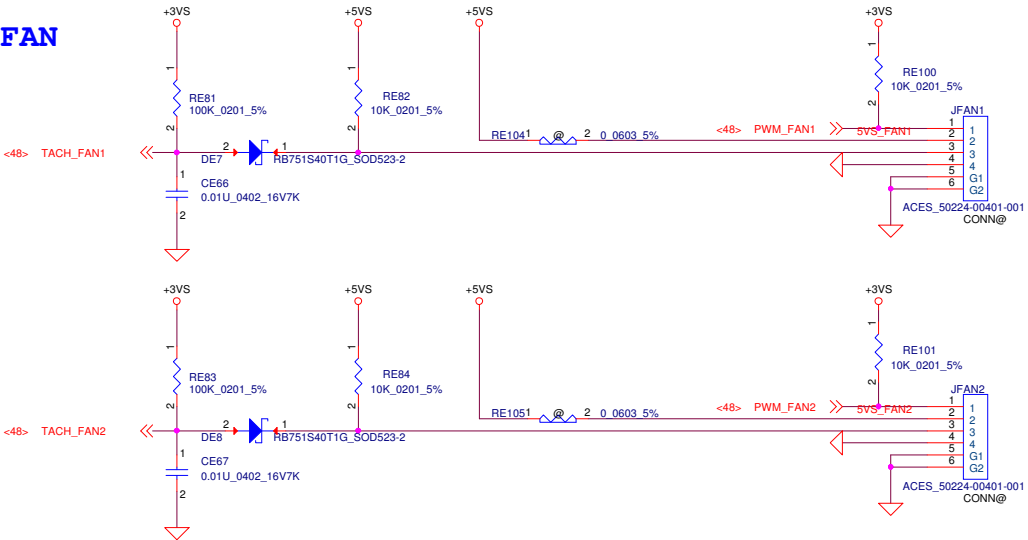


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Size	Document Number	Rev	Date	
Custom	LA-G341P	1.0/000	Wednesday, June 06, 2018	
Sheet		40	of	
Date		1	Sheet	

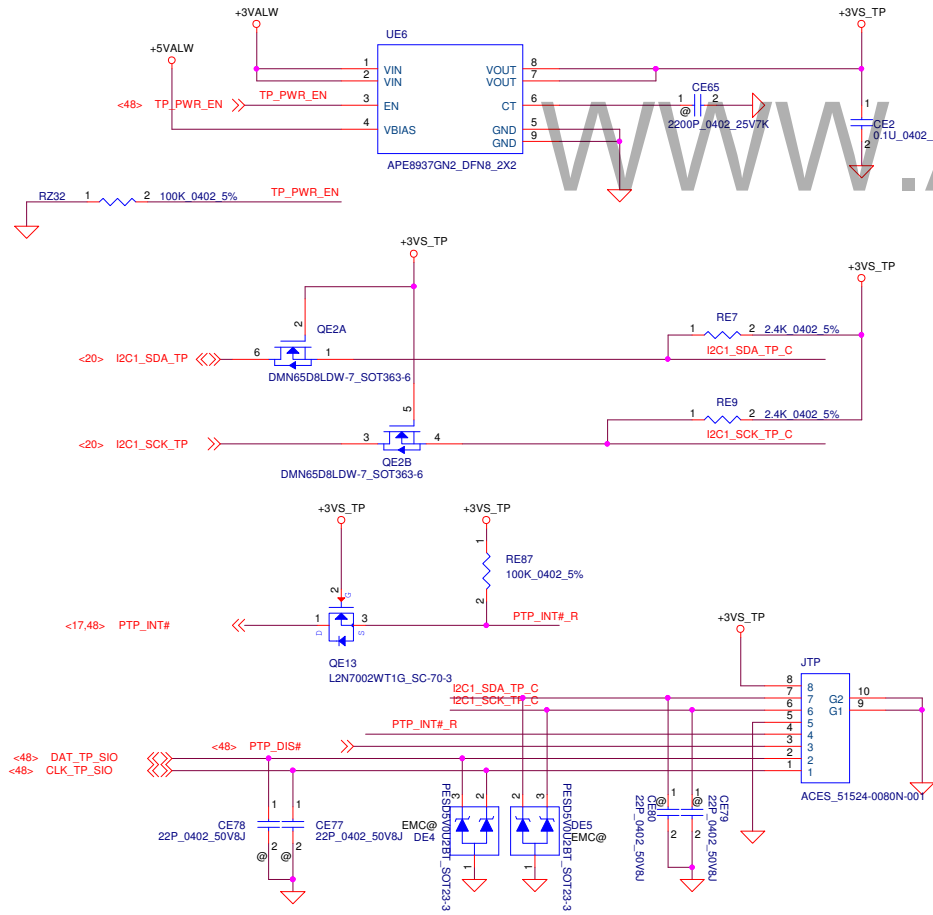
Power Button and LED



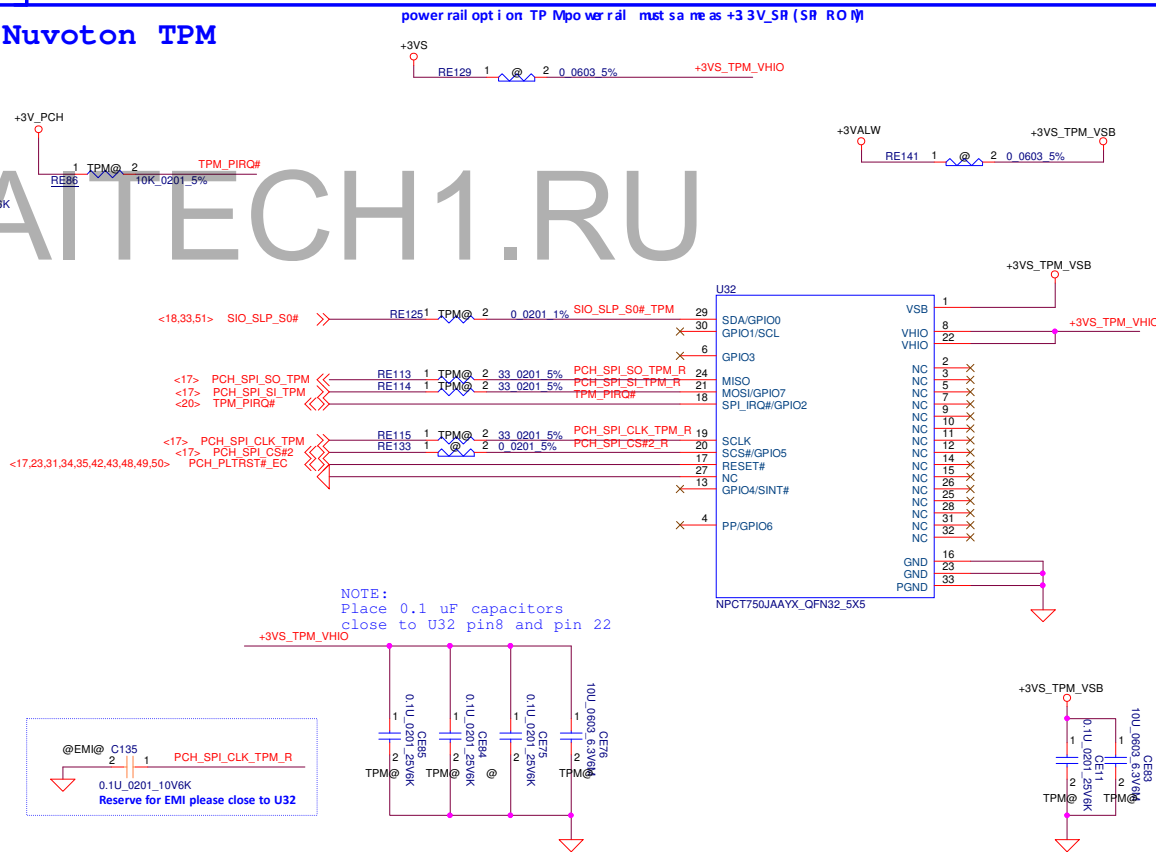
PWM FAN



Touch pad

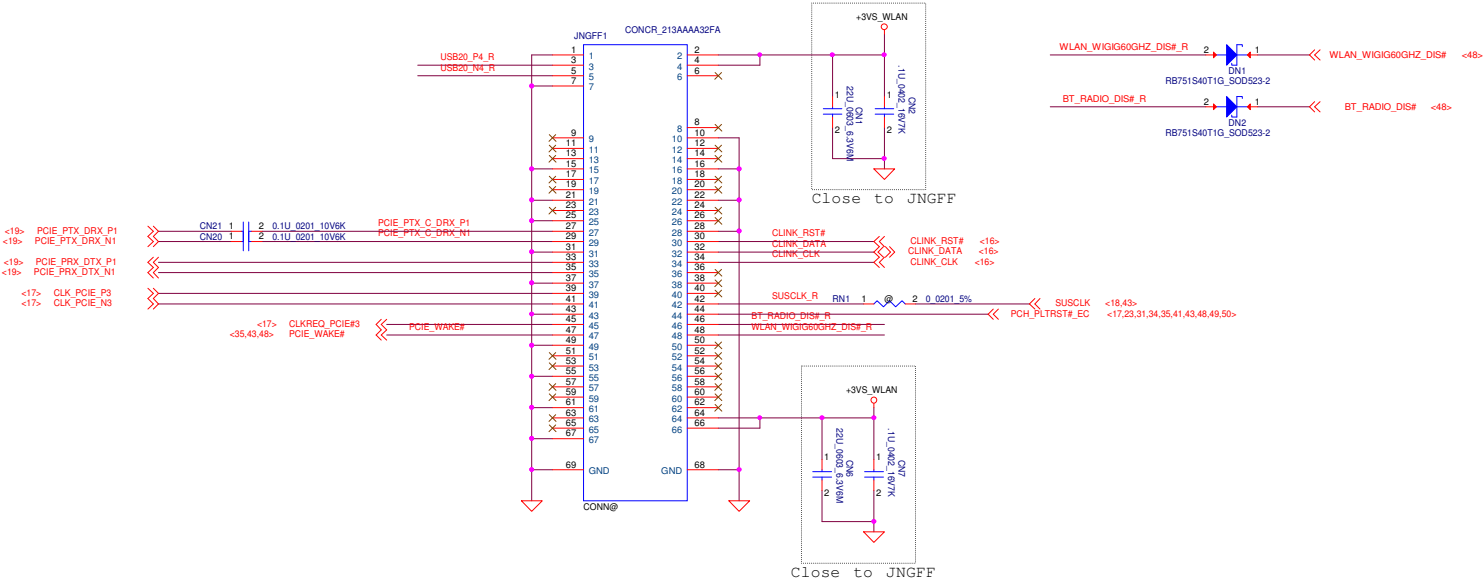


Nuvoton TPM

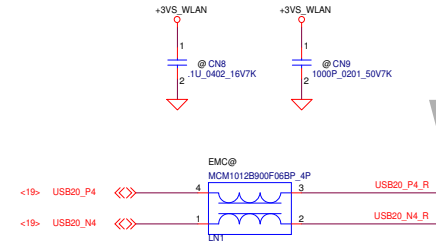


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Size	Document	Number	Rev	1.0(400)	
Custom	LA-G31P				
Date:	Wednesday, June 06, 2018	Sheet	41 of 76		

M.2 Slot-A Key-A (WLAN + BT)



Reserve for EMI



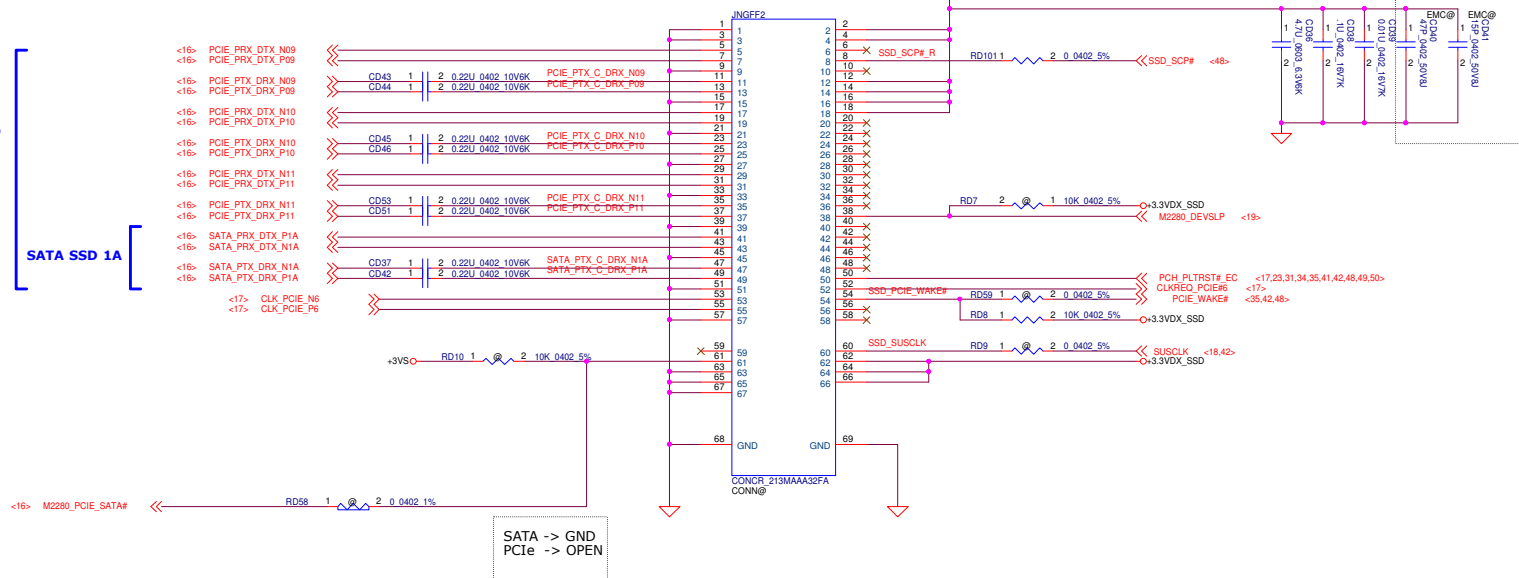
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Size	Document Number	Rev		1.0(00)
C	LA-G341P			
Date:	Wednesday, June 06, 2018	Sheet	42	of 76

# M.2 Slot-C Key-M (SSD)

PCIe SSD

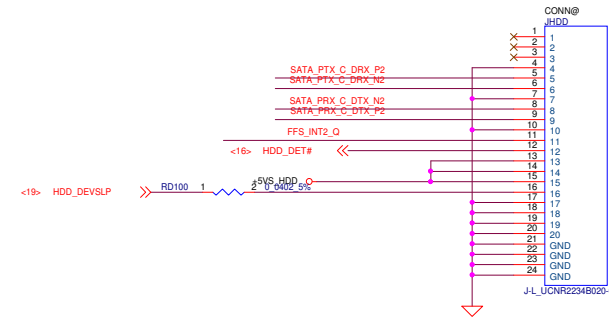
SATA SSD 1A



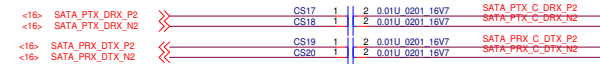
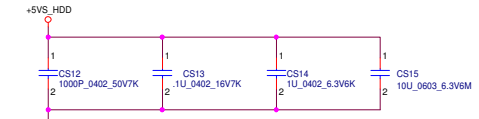
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Issued Date	2017/06/21	Deciphered Date	2027/06/21	Title	
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Size	Document Number	Rev		1.0(00)	
C	LA-G341P				
Date:	Wednesday, June 06, 2018	Sheet	43	of	76



## HDD CONN

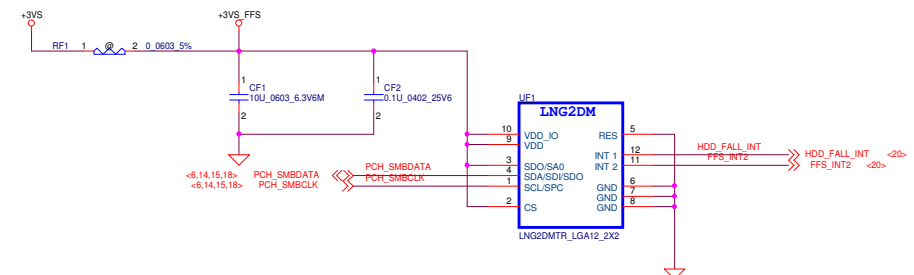
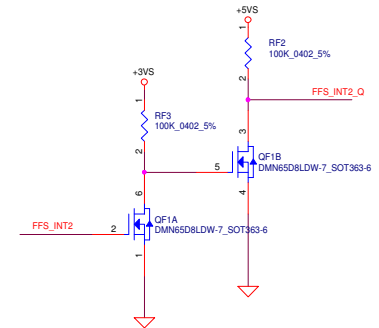
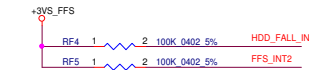


Place near HDD CONN (JHDD1)



## BYPASS Circuit

## Free Fall Sensor

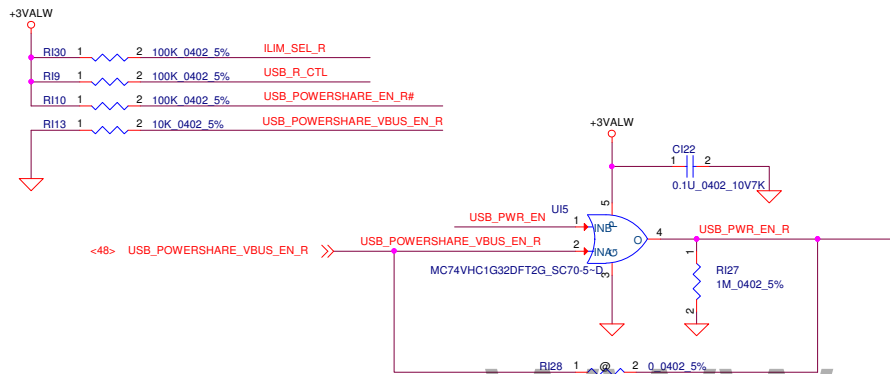


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				Document Number
				LA-G341P
				Rev
				1.0/000
				Date: Wednesday, June 06, 2018
				Sheet 44 of 76

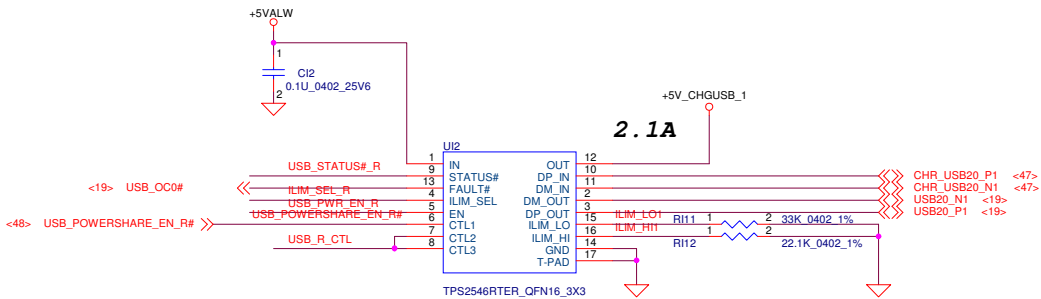
USB Powershare

Device Control Pins				Flow Line Condition
CTL1	CTL2	CTL3	ILIM_SEL	
0	1	1	X	DCP AUTO
1	1	1	0	SDP
1	1	1	1	CDP

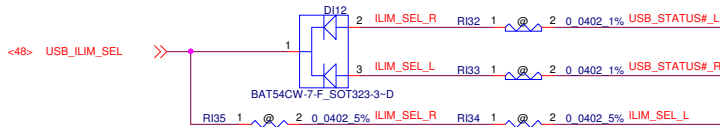
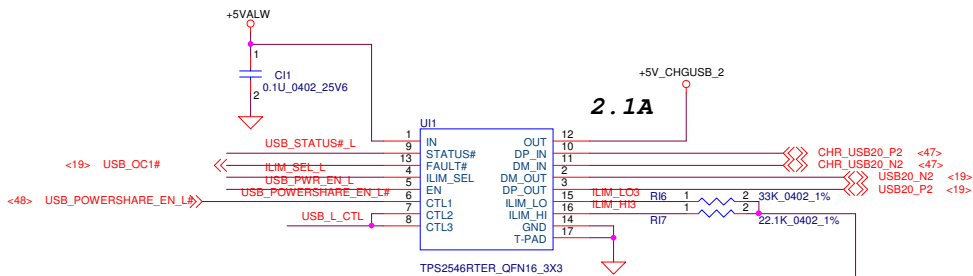
Suspend mode	CTL1 = 0 : Enable Power Share DCP mode in Suspend mode
	CTL1 = 1 : Disable Power Share in Suspend mode (For Support USB wake)
S0 mode	ILIM_SEL = 0 : SDP mode (0.9A by ILIM_LO setting)
	ILIM_SEL = 1 : CDP mode (STATUS# trigger by ILIM_HI =2.2A)

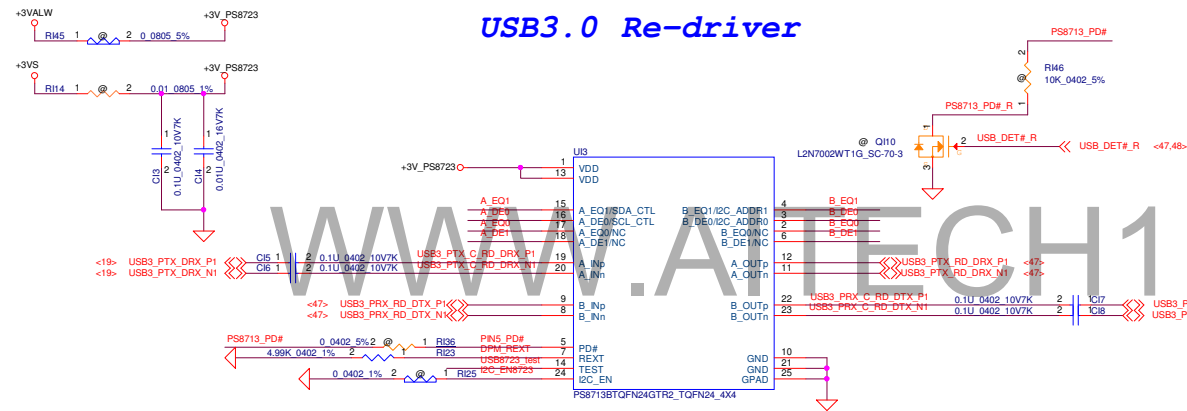


USB3.1 / USB2.0 Port1 (Right Side)



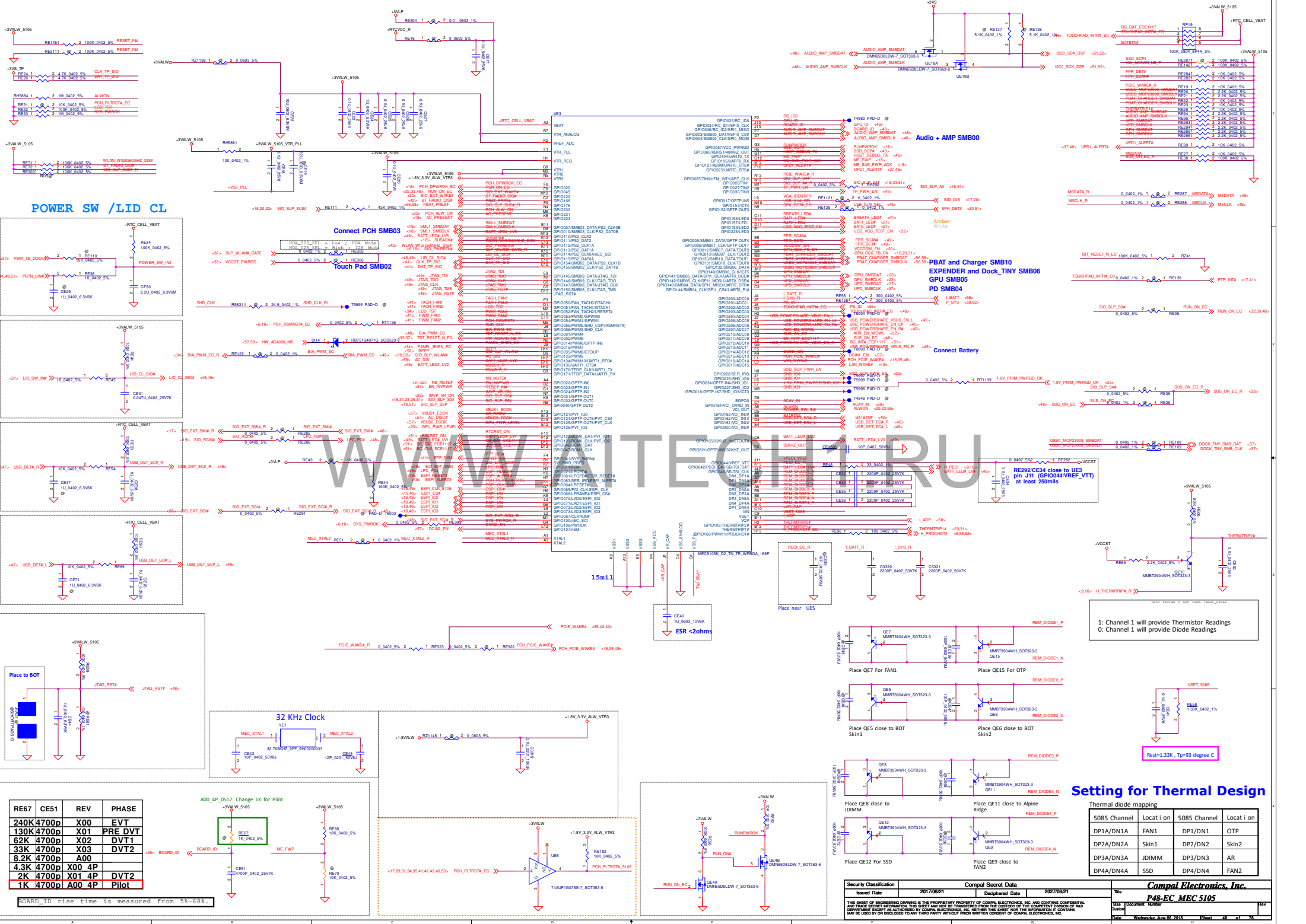
USB3.1 / USB2.0 Port2 (Left Side)



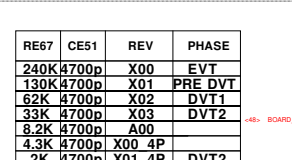
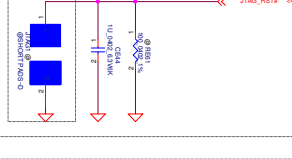
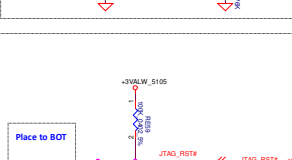
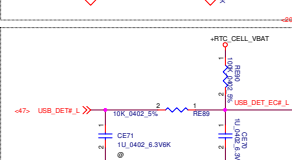
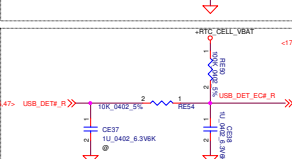
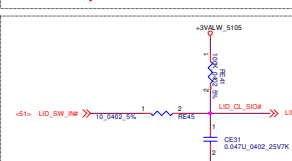
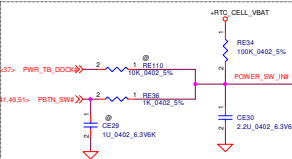
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				P46-USB3.1 retimer	
				Size	
				Document Number	
				Rev	
				1.0/000	
				Date: Wednesday, June 06, 2018	
				Sheet 46 of 76	





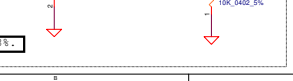
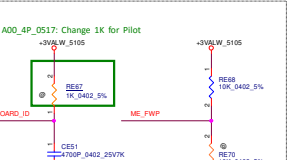
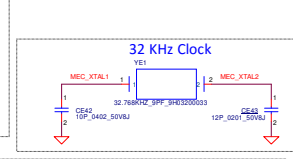
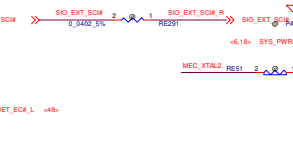
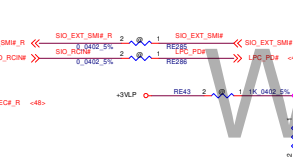
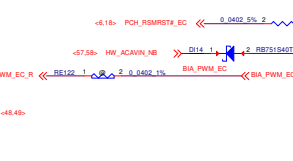
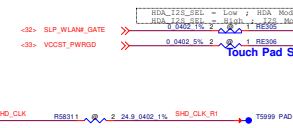
# POWER SW /LID CL



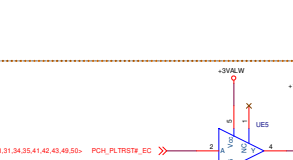
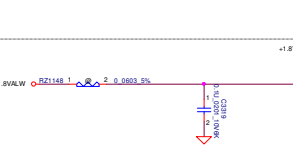
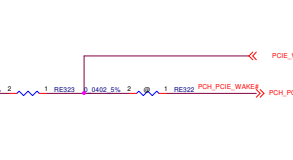
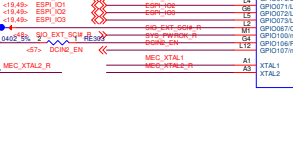
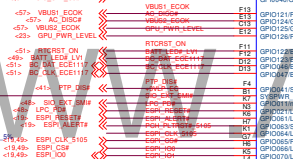
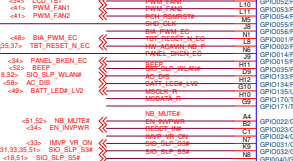
RE67	CE51	REV	PHASE
240K 4700p	X00	EVT	
130K 4700p	X01	PRE DVT	
62K 4700p	X02	DVT1	
33K 4700p	X03	DVT2	
8.2K 4700p	A00		
4.3K 4700p	X00 4P		
2K 4700p	X01 4P	DVT2	
1K 4700p	A00 4P	Pilot	

BOARD\_ID rise time is measured from 5%-68%.

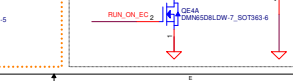
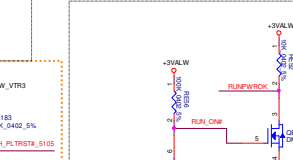
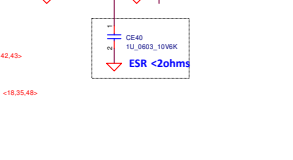
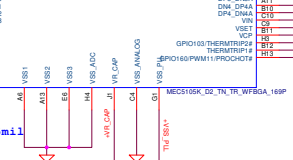
# Audio + AMP SMB00



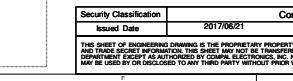
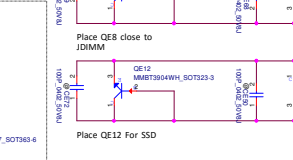
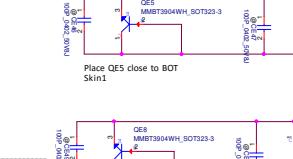
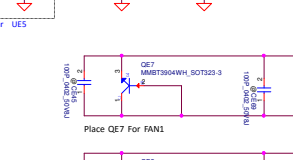
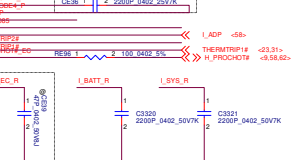
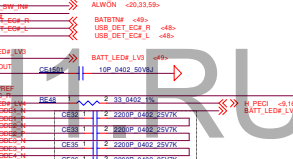
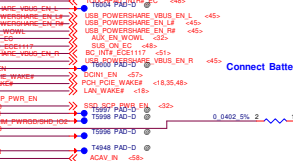
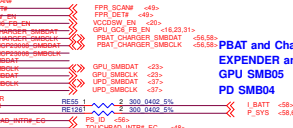
# PBAT and Charger SMB10



# Connect Battery



# Setting for Thermal Design



# Thermal diode mapping

5085 Channel	Locat i on	5085 Channel	Locat i on
DP1A/DN1A	FAN1	DP1/DN1	OTP
DP2A/DN2A	Skin1	DP2/DN2	Skin2
DP3A/DN3A	JDIMM	DP3/DN3	AR
DP4A/DN4A	SSD	DP4/DN4	FAN2

RE67	CE51	REV	PHASE
240K 4700p	X00	EVT	
130K 4700p	X01	PRE DVT	
62K 4700p	X02	DVT1	
33K 4700p	X03	DVT2	
8.2K 4700p	A00		
4.3K 4700p	X00 4P		
2K 4700p	X01 4P	DVT2	
1K 4700p	A00 4P	Pilot	

BOARD\_ID rise time is measured from 5%-68%.

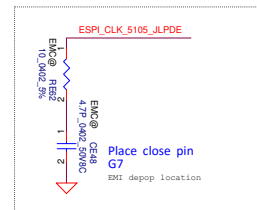
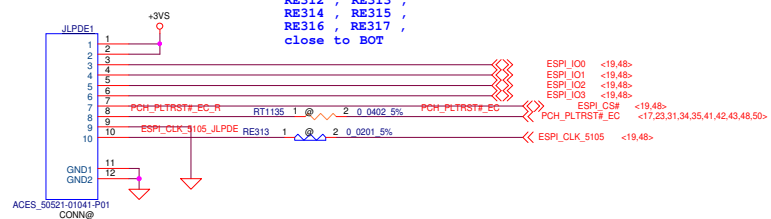
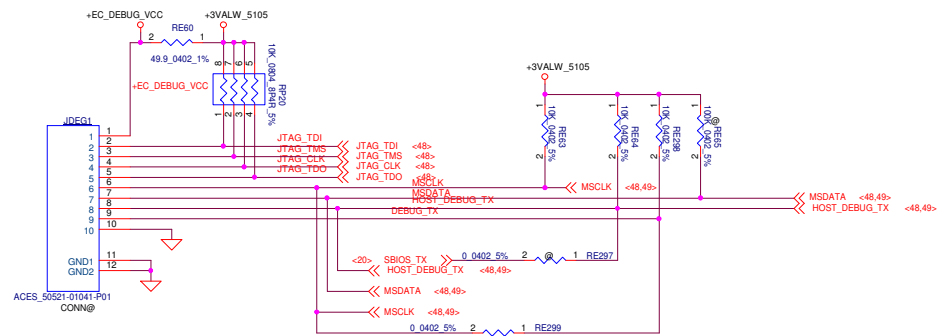
Rest+1.33K, T+93 degree C

1: Channel 1 will provide Thermistor Readings  
0: Channel 1 will provide Diode Readings

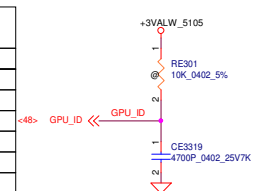
Compal Electronics, Inc.  
P48-EC MEC 5105

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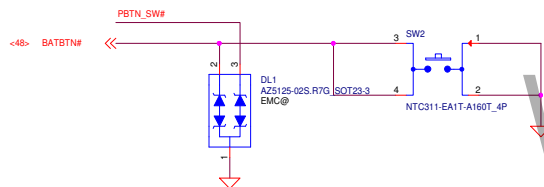
Issued Date: 2017/06/21  
Deciphered Date: 2027/06/21  
Title: P48-EC MEC 5105  
Date: Wednesday, June 26, 2018  
Page: 68 of 78



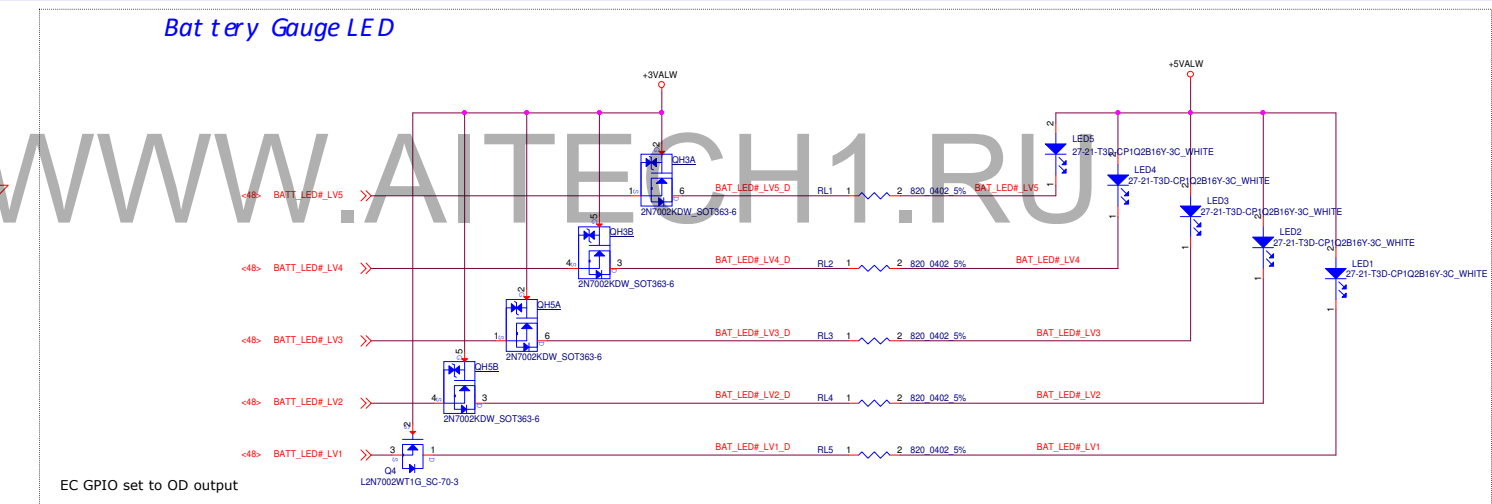
RE301	CE3319	REV
240K	4700p	i3 CPU/UMA
130K	4700p	UMA
62K	4700p	N17P-G0
33K	4700p	N17P-G1
8.2K	4700p	N18P-Q1
4.3K	4700p	N18P-Q3
2K	4700p	
1K	4700p	



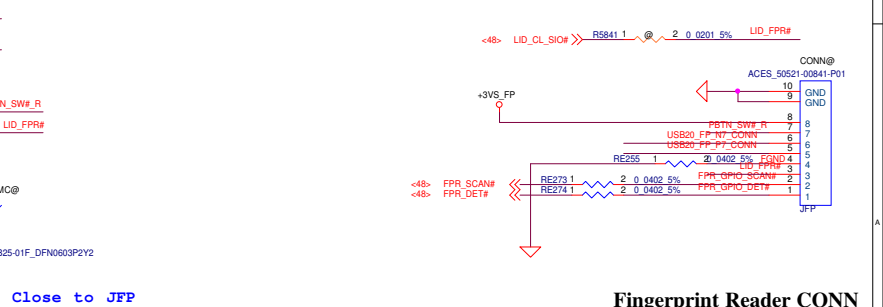
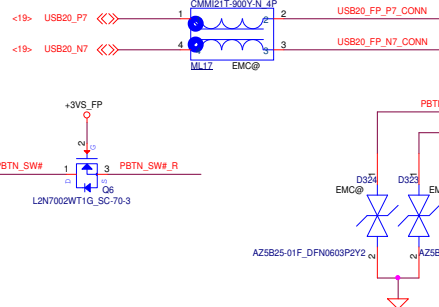
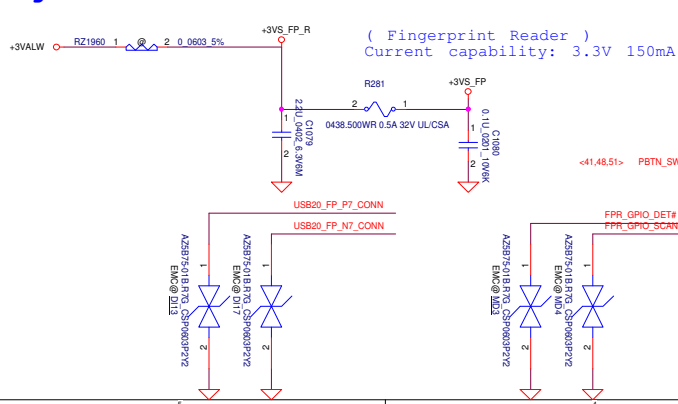
## BATT LED Power Button



### Bat tery Gauge LED



## Finger Print circuit

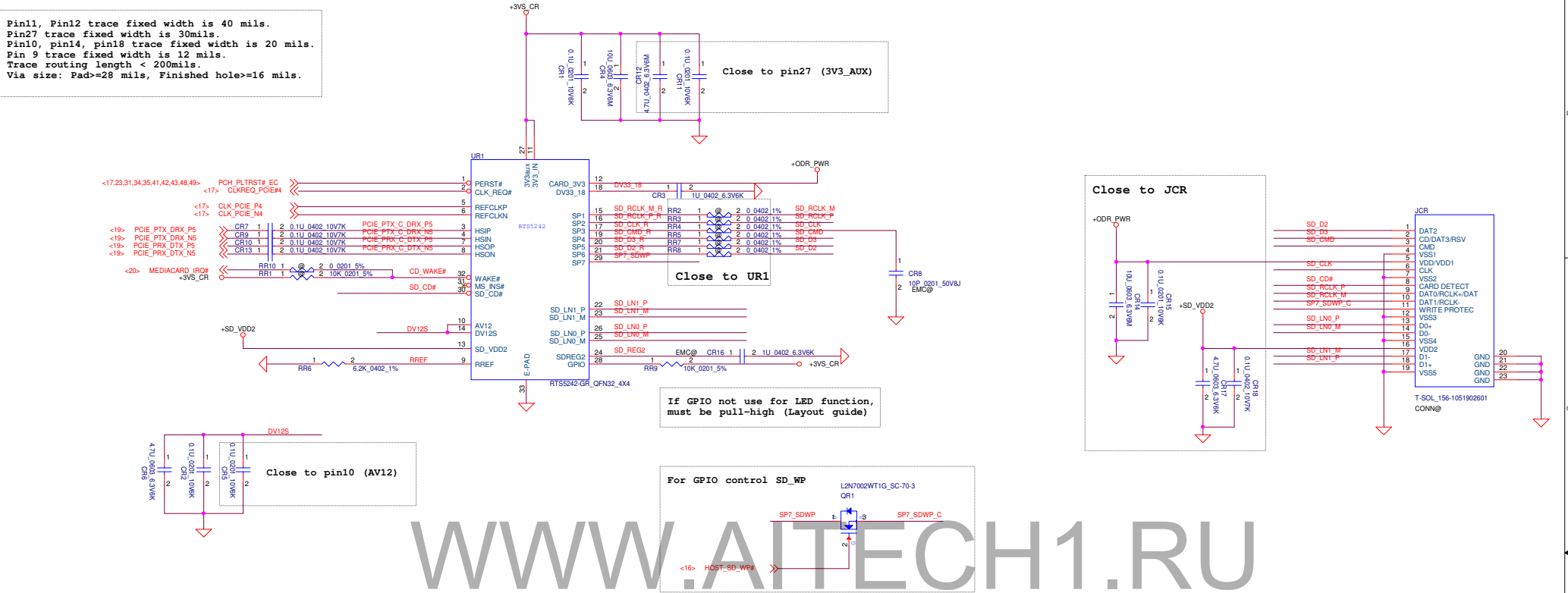


### Fingerprint Reader CONN

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					LA-G341P	1.0/1000
				Date:	Wednesday, June 06, 2018	Sheet

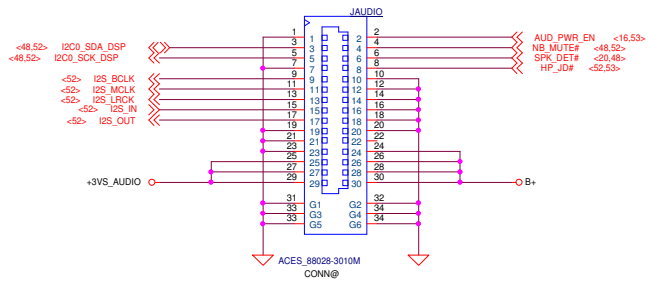
Card Reader

Pin11, Pin12 trace fixed width is 40 mils.  
Pin27 trace fixed width is 30mils.  
Pin10, pin14, pin18 trace fixed width is 20 mils.  
Pin 9 trace fixed width is 12 mils.  
Trace routing length < 200mils.  
Via size: Pad>=28 mils, Finished hole>=16 mils.

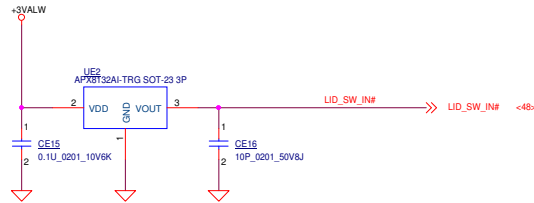




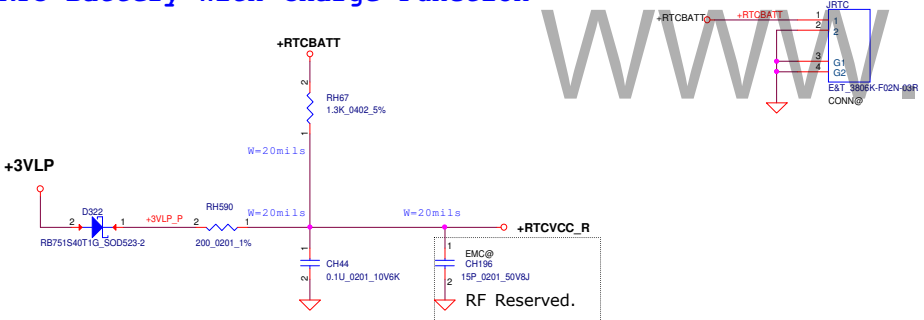
## AUDIO Board Conn.



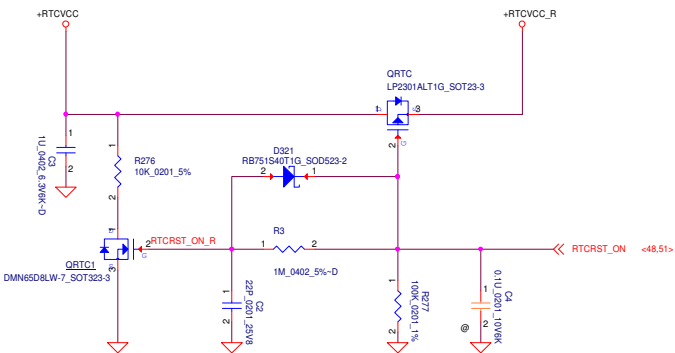
## Lid Switch



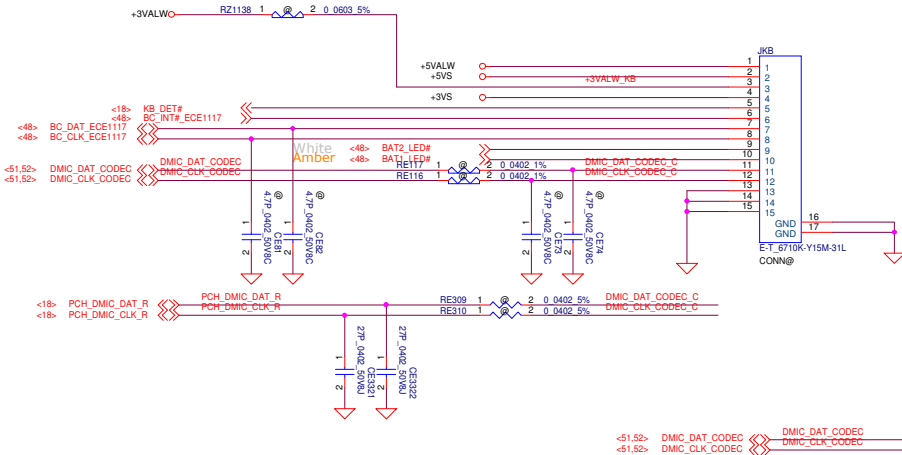
## RTC Battery With Charge Function



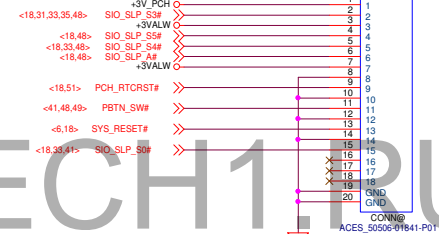
Default: OD EC drives GPIOs to LOW to turn off power to VCCRTC.



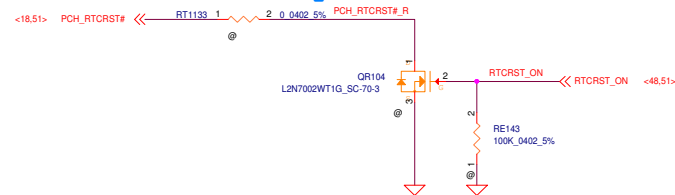
## Keyboard Controller board + DMIC



### APS CONN



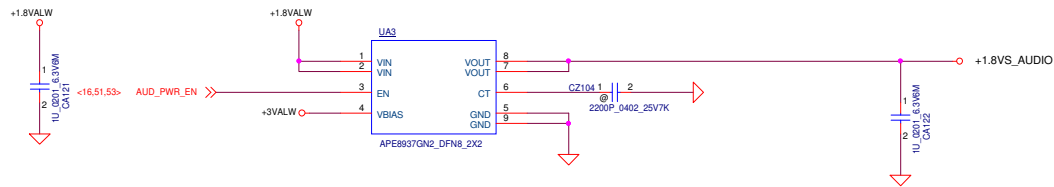
## follow Intel Keep old RTC



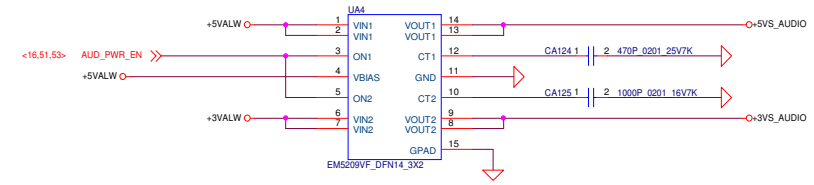
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Issued Date	2017/06/21	Deciphered Date	2027/06/21	Title	
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				Size	Document Number
				LA-G341P	
				Date:	Wednesday, June 06, 2018
				Sheet	51 of 76
				Rev	1.0/000



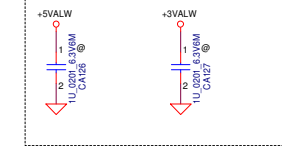
## +1.8VALW To +1.8VS\_AUDIO



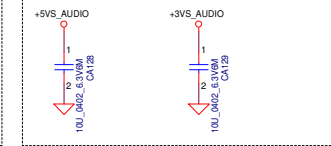
## +5VALW and +3VALW To +5VS\_AUDIO and +3VS\_AUDIO



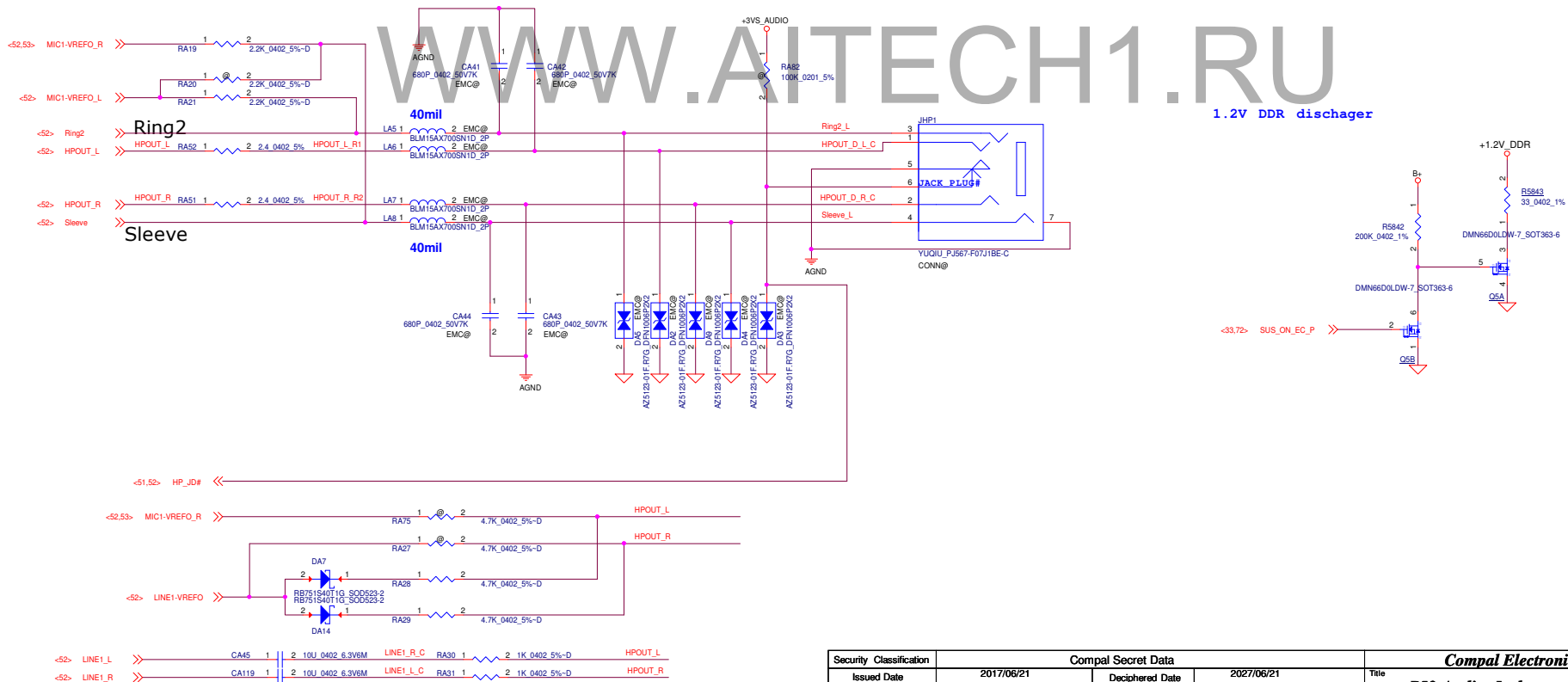
Close UA4



Close UA4

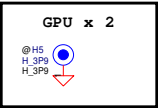
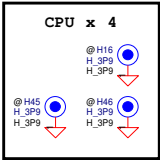


## Universal Audio Jack

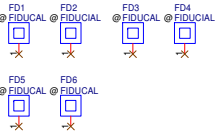
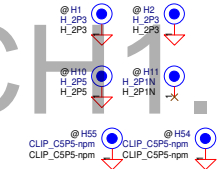
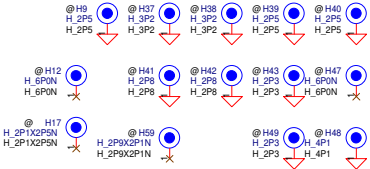
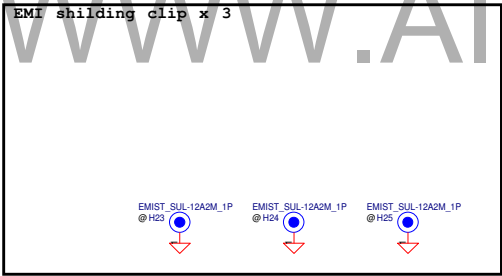
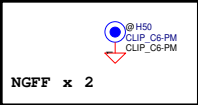


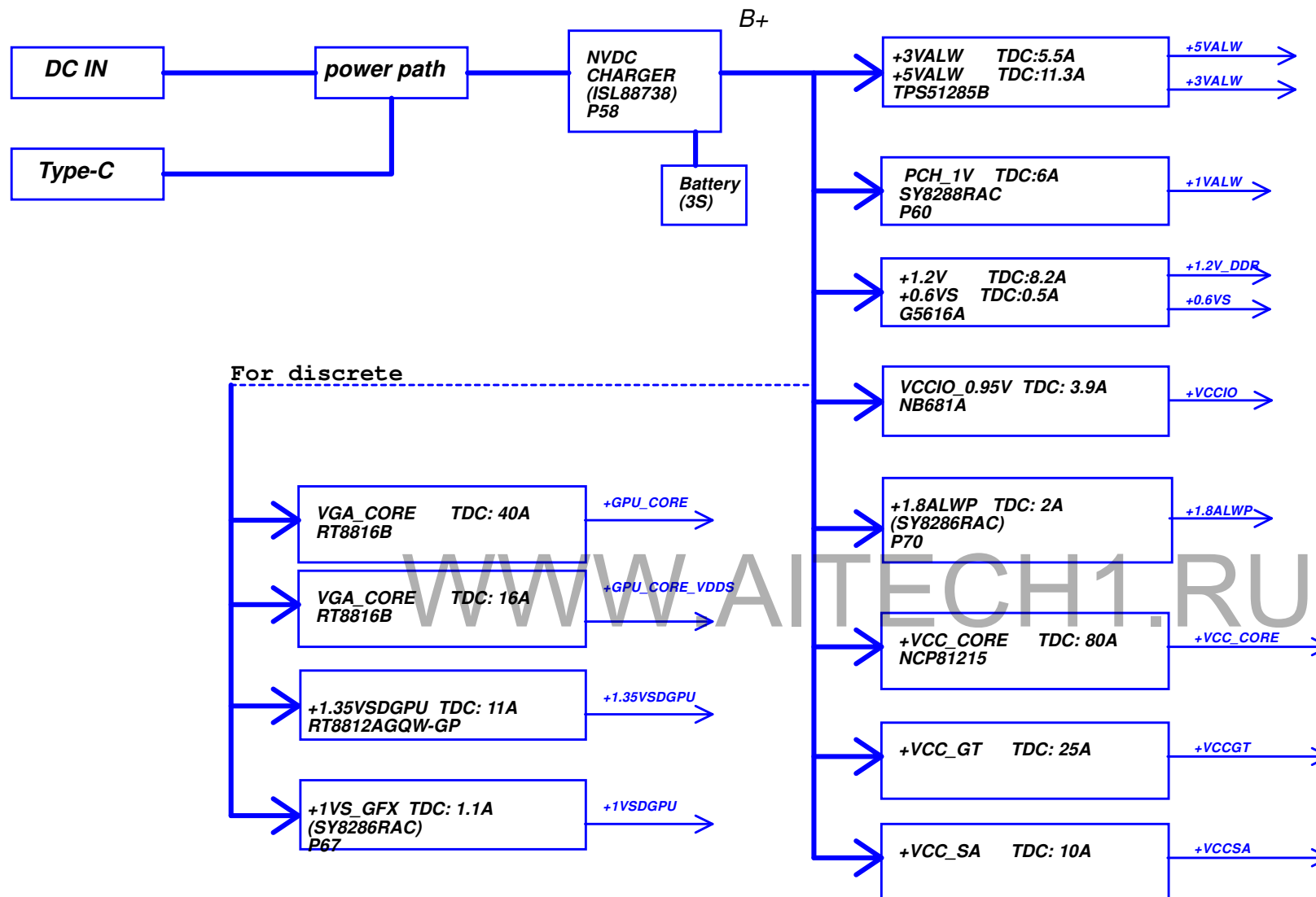
Security Classification	Compal Secret Data		Title	
Issued Date	2017/06/21	Deciphered Date	2027/06/21	Size
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				LA-G341P
				Rev 1.0/000
				Date: Wednesday, June 06, 2018
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Screw Hole

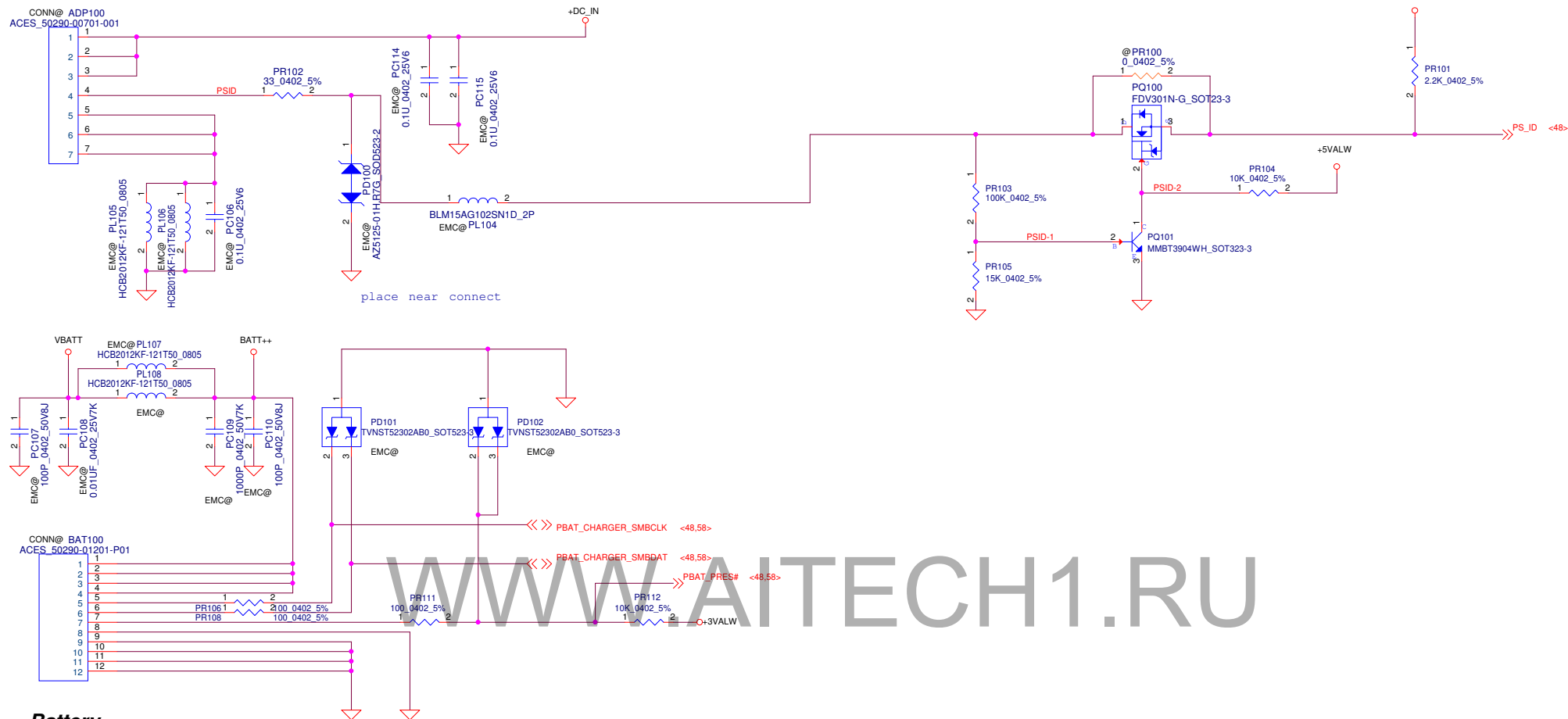


X03\_1222: for peel off issue,  
change footprint to CLIP\_C6-PM





@ : Nopop Component  
 @DIS@ : Nopop Component  
 DIS@: POP for discrete GPU SKU



**Battery**  
**(3S2P) 97W**  
**(3S1P) 56W**

**JIMBTY battery connector**

**SMART**  
**Battery:**  
**01.BAT+**  
**02.BAT+**  
**03.BAT+**  
**04.BAT+**  
**05.CLK\_SMB**  
**06.DAT\_SMB**  
**07.BATT\_PRS**  
**08.SYS\_PRS**  
**09.GND**  
**10.GND**  
**11.GND**  
**12.GND**

Smart Adapter circuit (39.1)

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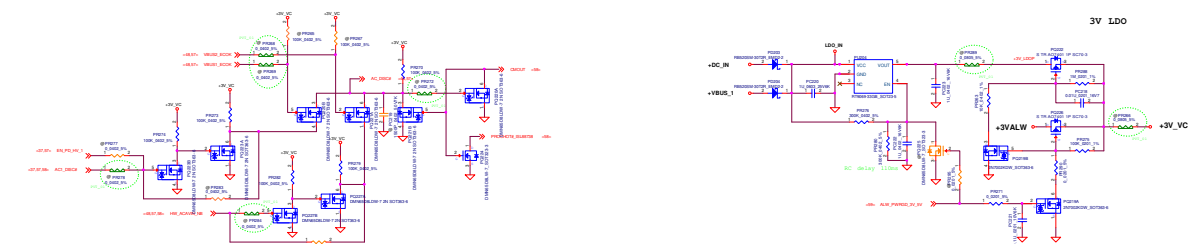
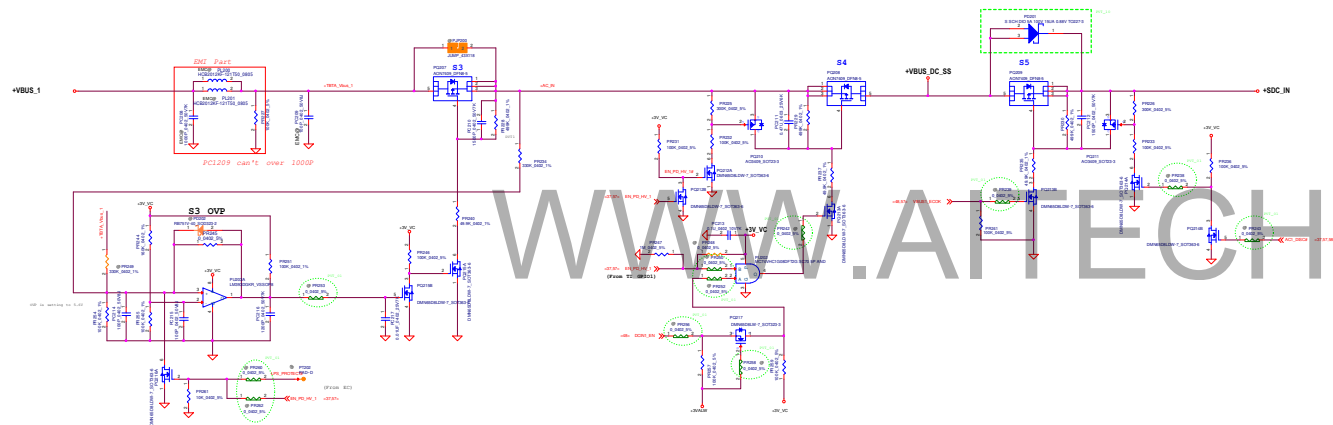
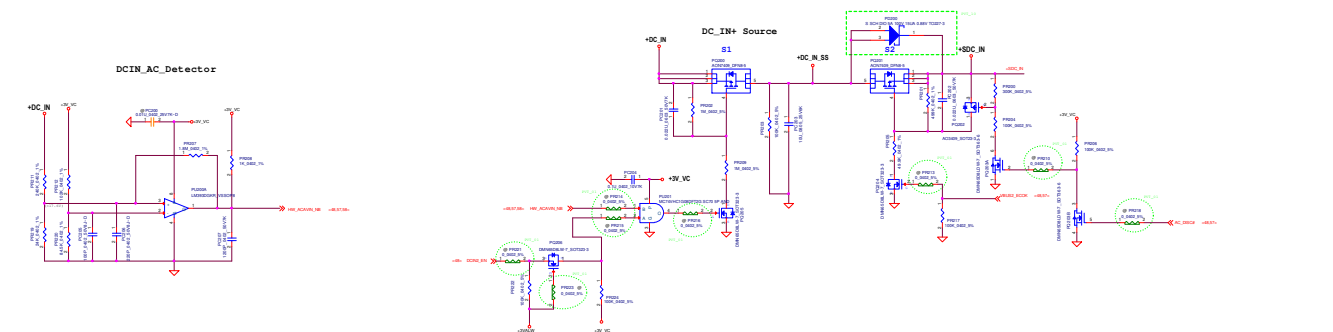
**Compal Electronics, Inc.**

**Title**  
**P56-PWR\_DCIN / BATT\_CONN / OTP**

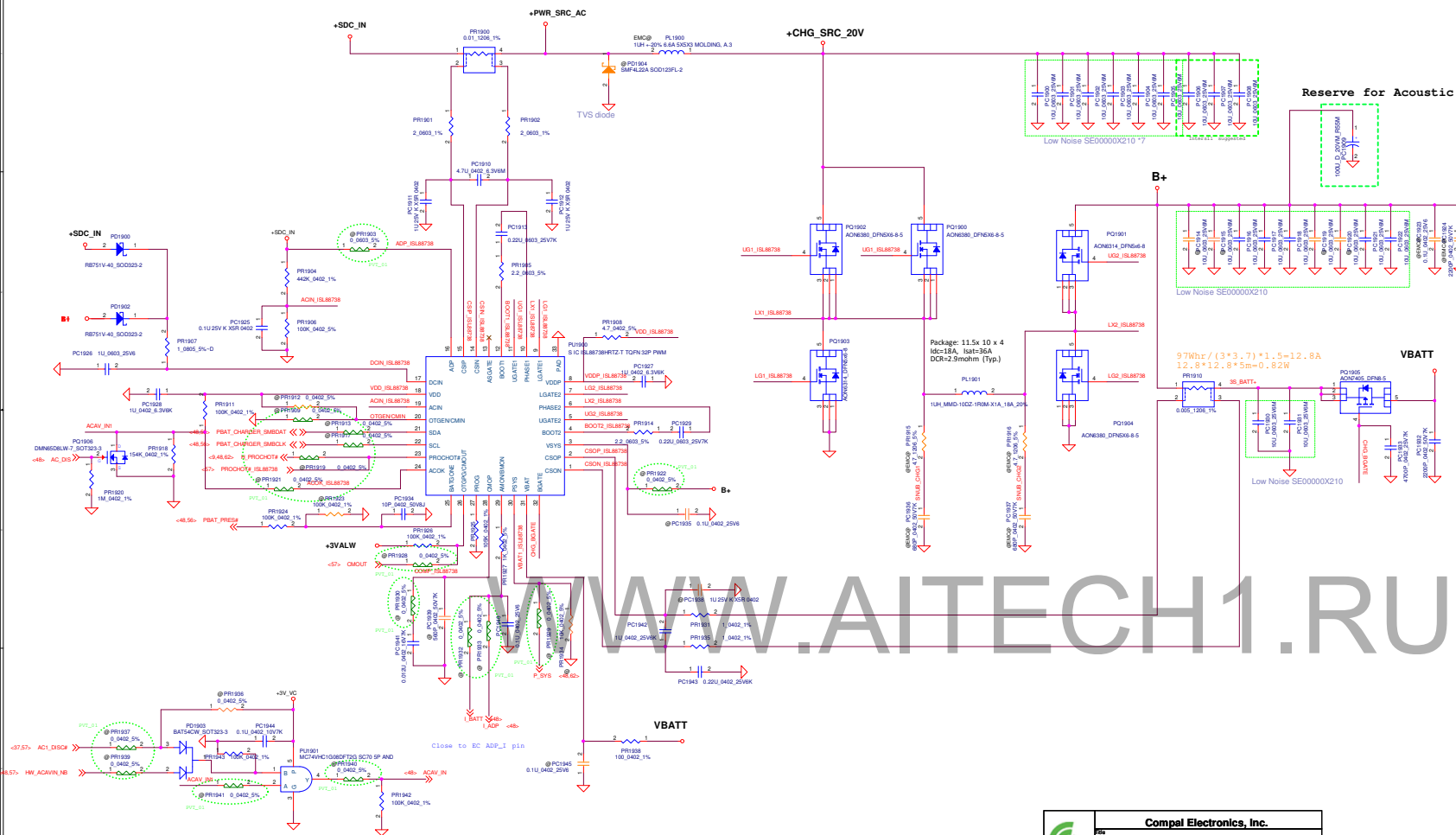
**Size**  
**Document Number**  
**LA-F541P**


**Rev**  
**0.1(00)**

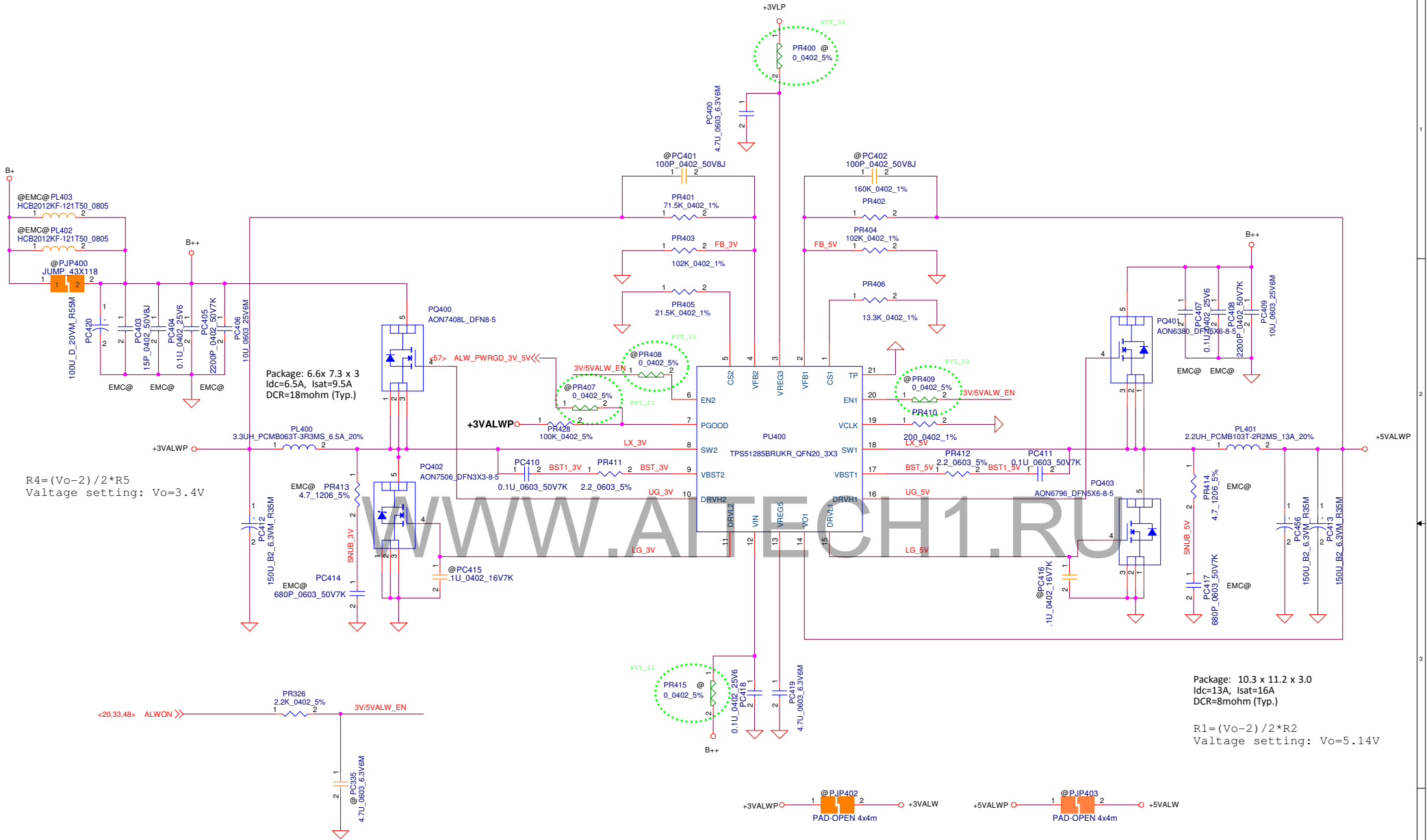
**Date:** Wednesday, June 06, 2018 **Sheet** 56 **of** 74







		Compal Electronics, Inc.	
		P58-PWR CHARGER (ISL88738)	
Rev	1	Document Number	LA-F541P
Date	Wednesday, June 06, 2018	Sheet	38 of 74



3.3VALWP  
 TDC 5.5A  
 Peak Current 7.7A  
 OCP current 9.35A

5VALWP  
 TDC 11.3A  
 Peak Current 12.6A  
 OCP current 19.2A

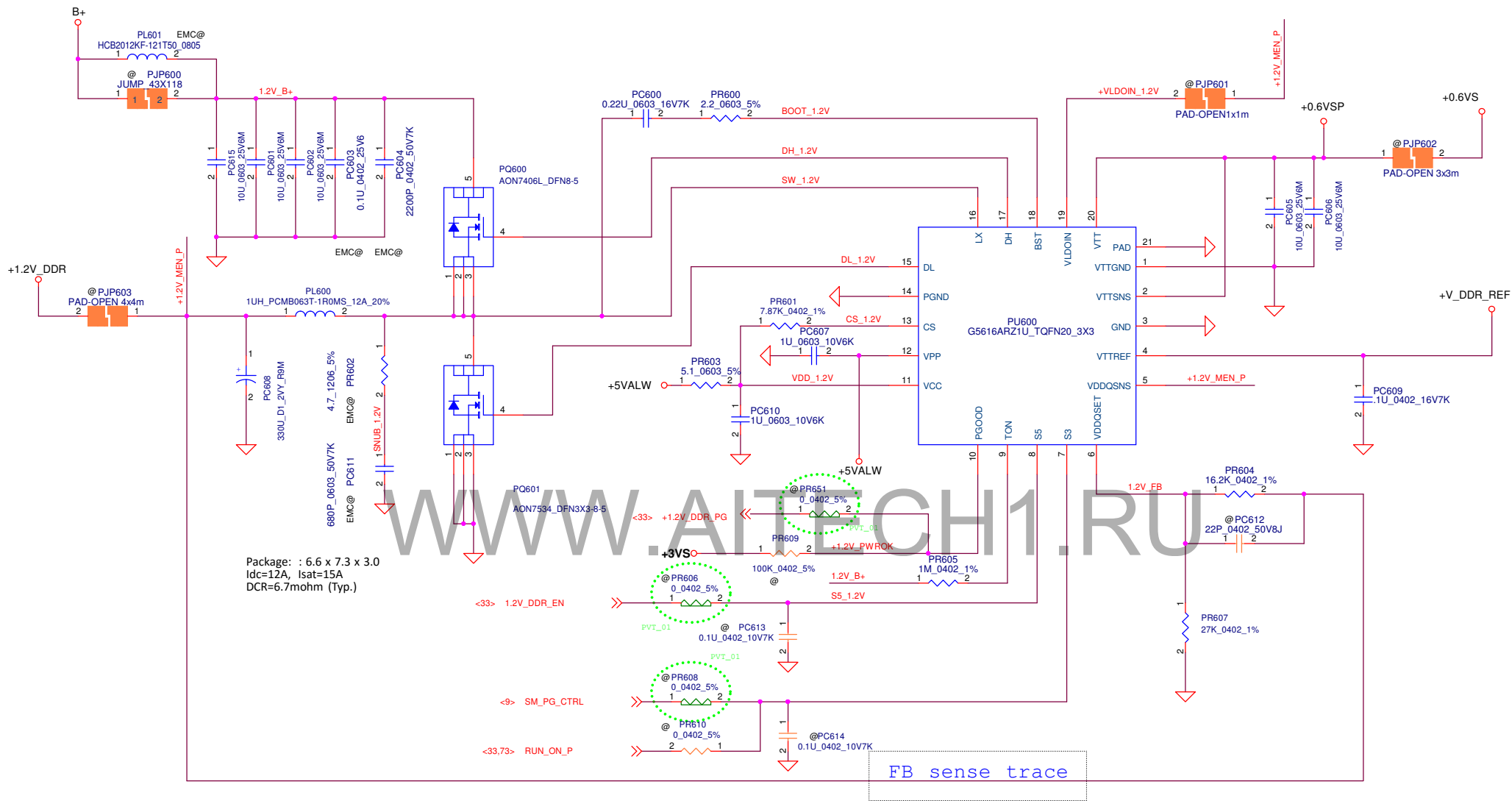
3V/5V controller(35.1), Support component(35.2)

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Compal Electronics, Inc.			
Title	P59-PWR 3.3VALWP/5VALWP		
Size	Document	Number	Rev
		LA-F541P	0.1(00)
Date:	Wednesday, June 06, 2018	Sheet	59 of 74



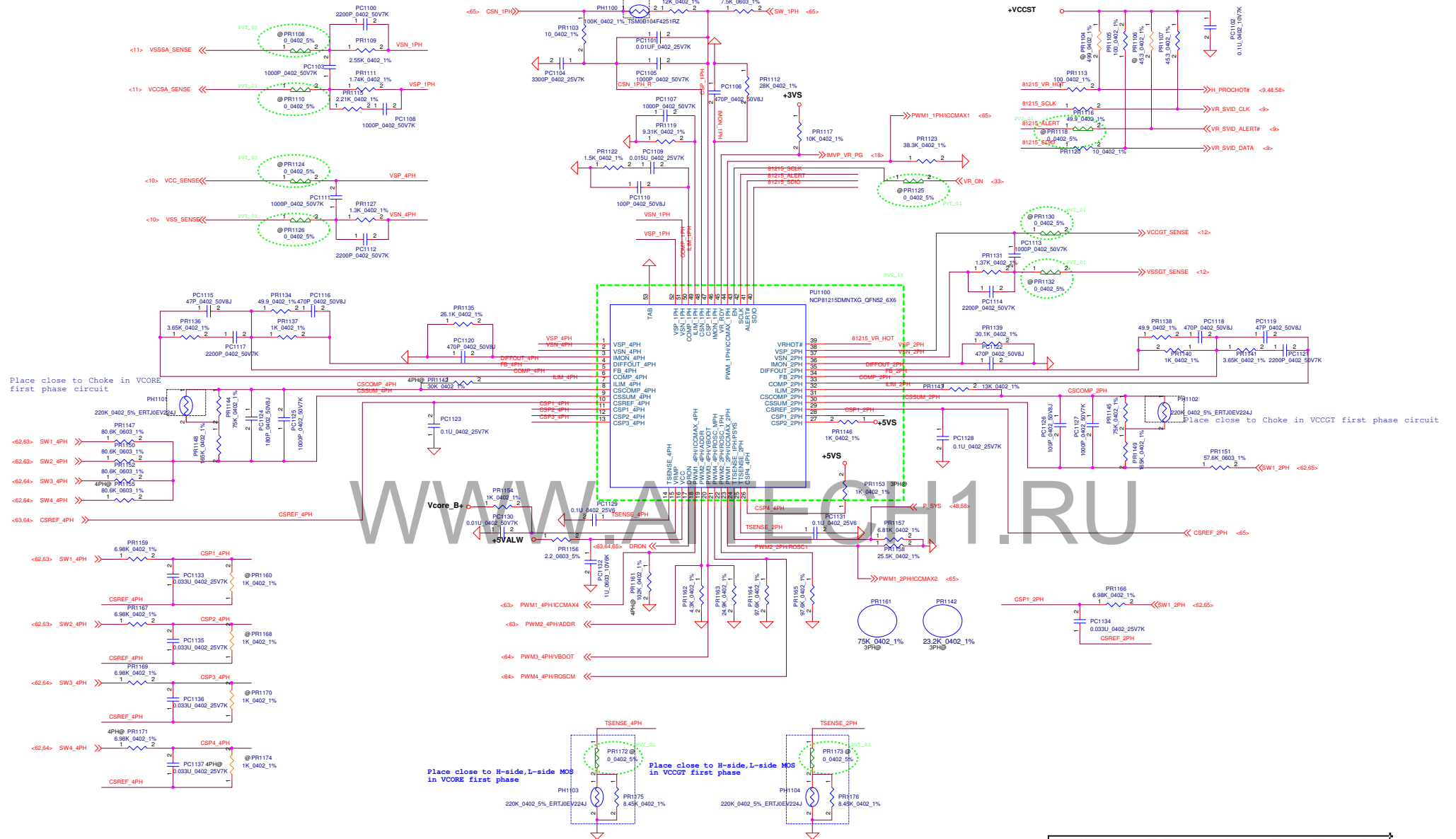


DDR controller(35.3), Support component(35.4)

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		<b>Compal Electronics, Inc.</b>	
		<b>Title</b> <b>P61-PWR +1.2V MEN/+0.6V DDR</b>	
<b>Size</b>	<b>Document Number</b>	<b>Rev</b> 0.1(000)	
<b>Date:</b> Wednesday, June 06, 2018		<b>Sheet</b> 61 <b>of</b> 74	

Place close to Choke in VCCSA first phase circuit



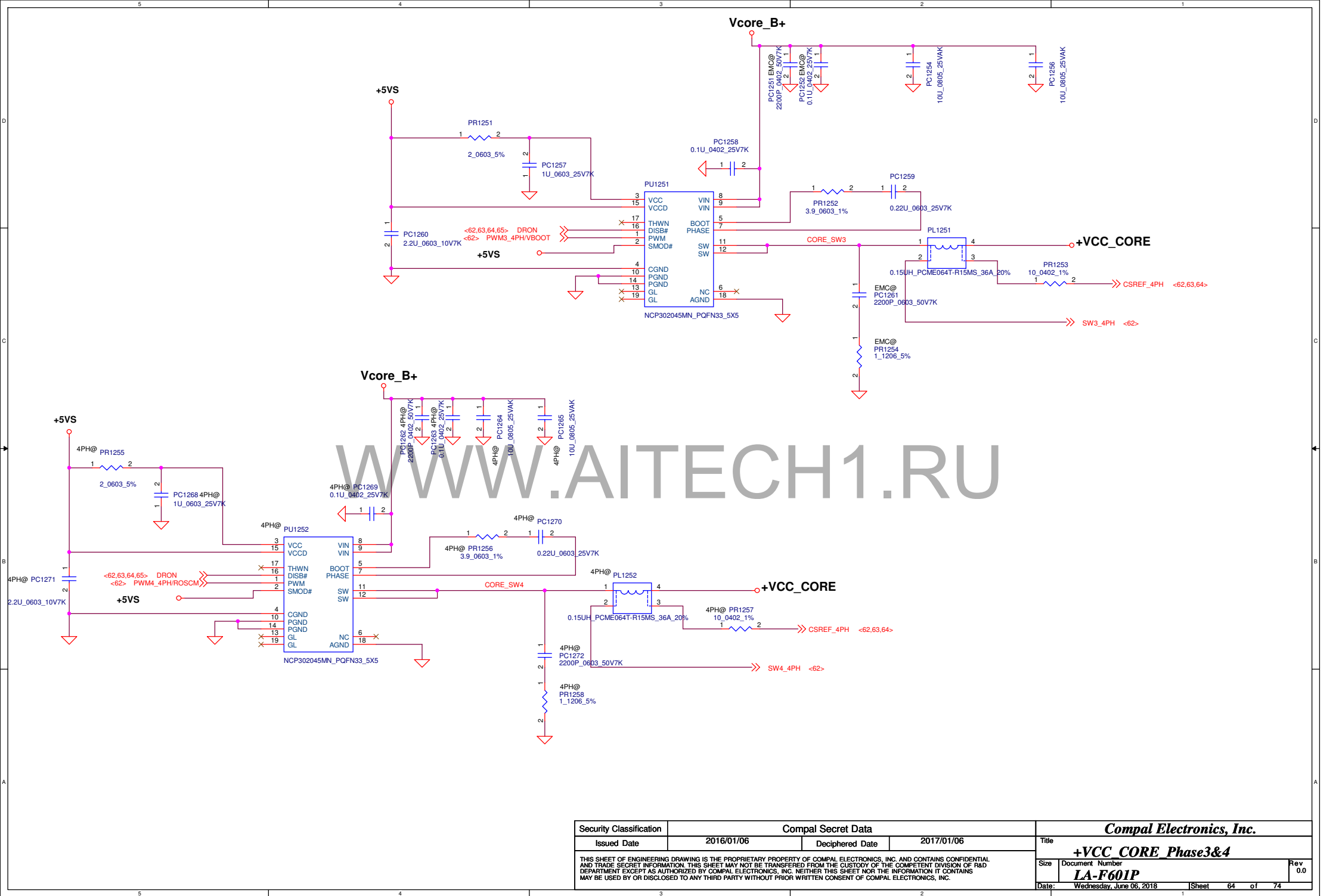
RAIL NAME	Enable	V <sub>IN</sub>	V <sub>OUT</sub>	I <sub>CCMax</sub>	I <sub>PL2</sub>
V <sub>CC</sub> (MVP8)	VR_EN	VDC	SVID	128.0 A	80.0 A
V <sub>CCGT</sub> (MVP8)	VR_EN	VDC	SVID	32.0 A	25.0 A
V <sub>CCSA</sub> (MVP8)	VR_EN	VDC	SVID	11.1 A	10.0 A

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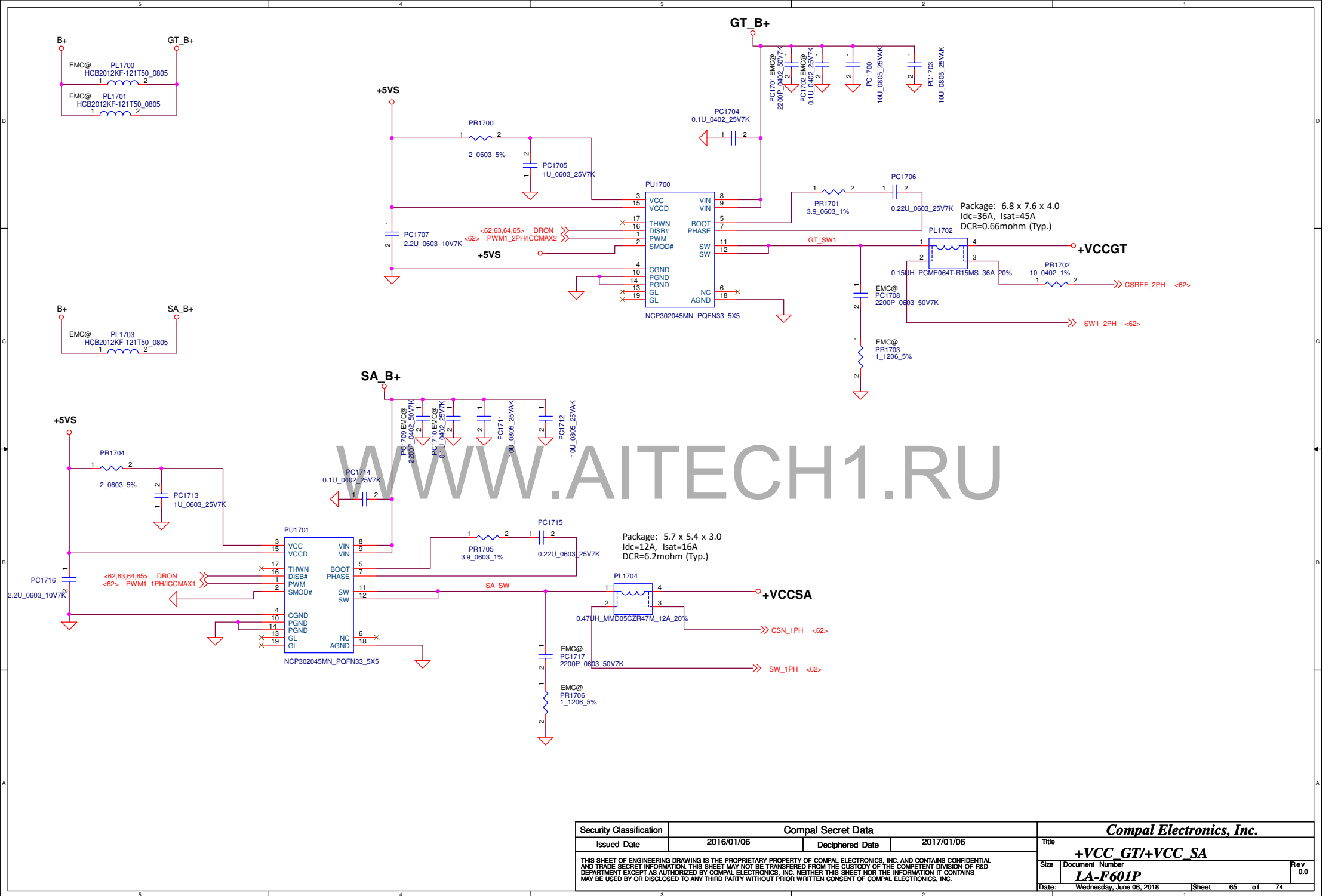
	Compal Electronics, Inc.			
	NCP81215			
	LA-F601P			
	Date: Wednesday, June 06, 2018	Sheet: 82	of: 74	Rev: 0.0





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				0.0	





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Size	Document Number	Rev		LA-F601P	
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+VCC\_CORE  
470uF\*2  
220uF\*1  
22uF\*40  
1uF\*24

PVT\_02

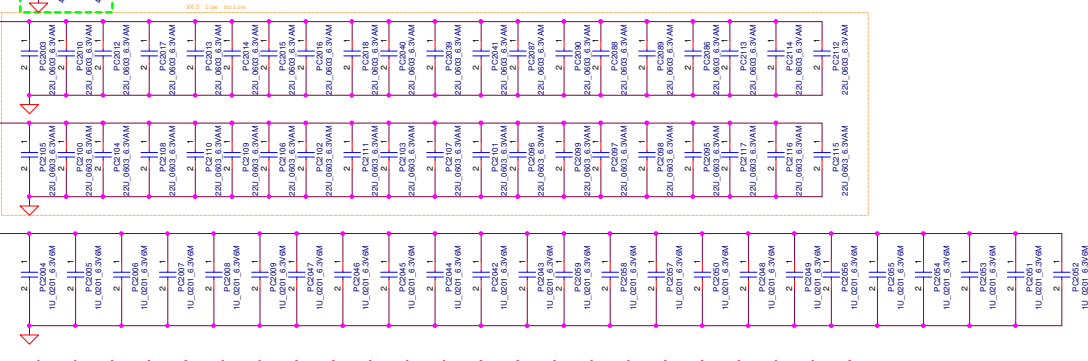
Vcc

5x 47uF 0805	12x 22uF 0603
	21x 10uF 0402
	24x 1uF 0201
	24x 0201 (placeholder)

Bulk Decoupling Locations

EXAMPLE

Vcc Power Plane at VR output	3x 220uF
Vccgr Power Plane at VR output	2x 220uF
Vccog Power Plane at VR output	2x 47uF 0805
Vccsa Power Plane at VR output	2x 47uF 0805

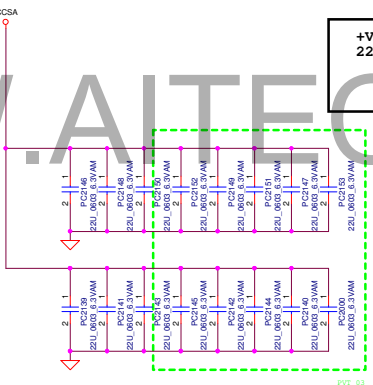


+VCCGT  
470uF\*2  
22uF\*32  
1uF\*12

VCCGT

3x 47uF 0805	
7x 22uF 0603	
10x 10uF 0402	
12x 1uF 0201	

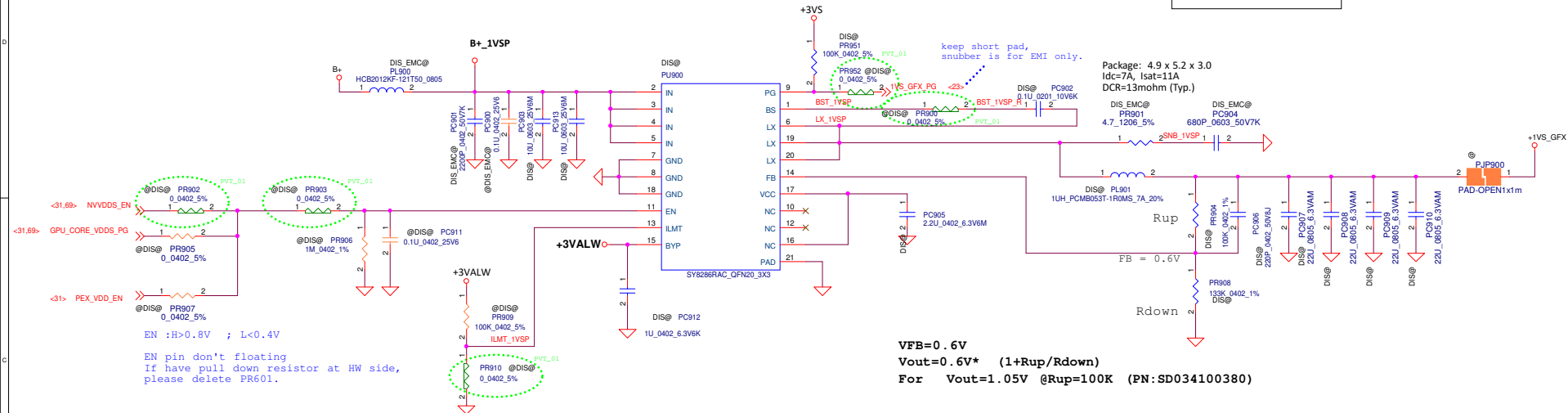
+VCCSA  
22uF\*16



Vccsa	2x 47uF 0805	
	2x 22uF 0603	
	7x 10uF 0402	

for dGPU SKU  
@DIS@ : Nopop Component  
DIS@: POP for dGPU SKU

+1.0VSP/1.05VSP  
TDC 1.1A  
Peak Current 1.1A  
OCP current 6A(fix)



WWW.AITECH1.RU

The current limit is set to 6A, 8A or 12A when this pin is pull low, floating or pull high

GPU other power\_Regulatorr(43.7), Support component(43.8)

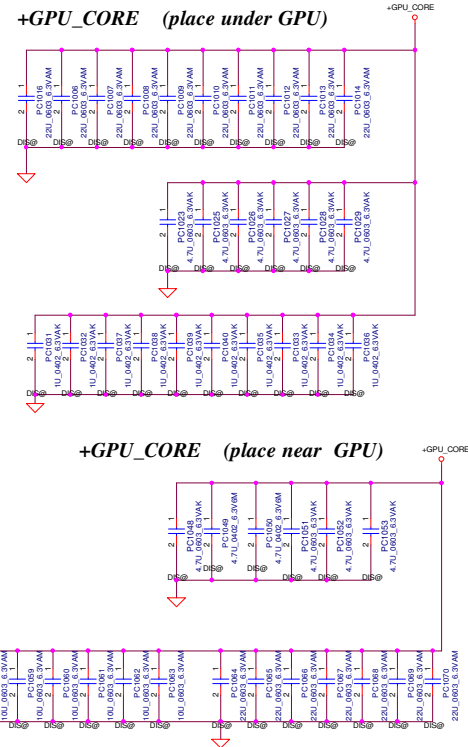
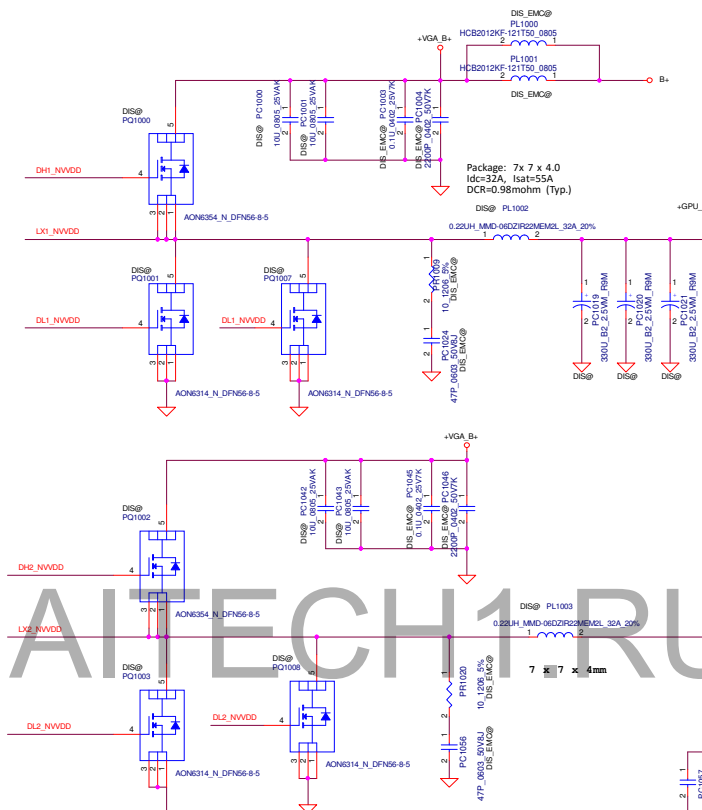
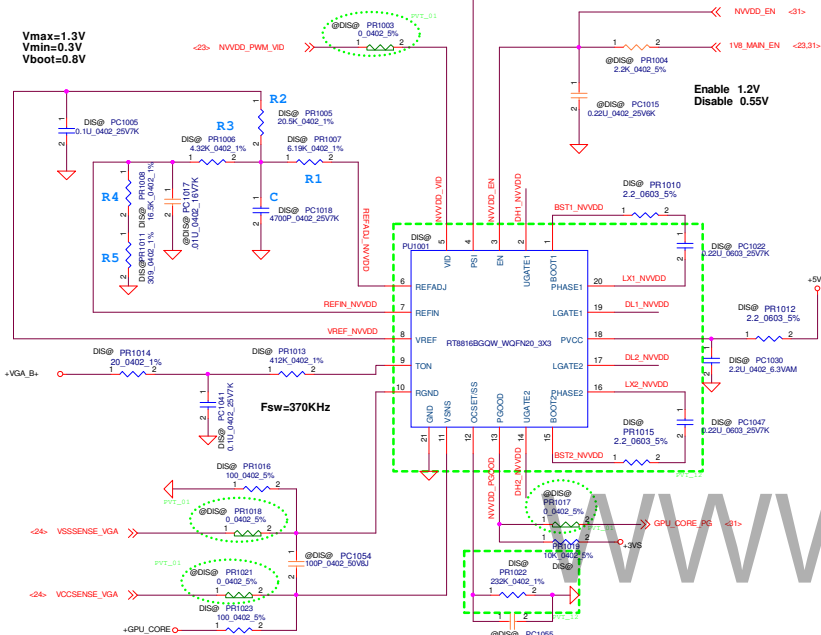
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Issued Date	2017/06/21	Deciphered Date	2027/06/21	Title	P67-PWR +1.05VSDGPU(SY8286RAC)
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```
for dGPU SKU
@DIS@ : Nopop Component
DIS@: POP for dGPU SKU
```

2phase with DEM	1.08V to 1.35V
2phase with CCM	1.6V to 5.5V

```
GPU_CORE (0.95V)
TDC 41A
Peak Current 94A
OCP current 100A
DCR 0.98mohm +/- 5%
```

	MIN	MAX
H/S Rds(on) :	4mohm	5.2mohm
L/S Rds(on) :	2.8mohm	3.5mohm



Under:  
4.7U\_0603\_6.3VAK \*16  
1U\_0402\_6.3VAK \*10


Near:  
10U\_0805\_6.3V6M\*7  
22U\_0805\_6.3V6M \*7  
4.7U\_0805\_6.3V6K \*6  
330u\*3

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- VGA\_CORE controller(43.1), Support component(43.2)
- VGA\_CORE Drivers (43.3), GPU Core Output CAP (43.9)

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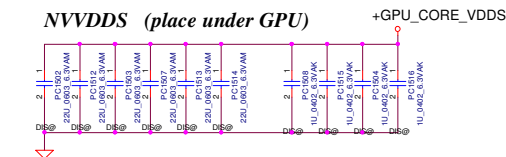
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	<b>Compal Electronics, Inc.</b>			
	<b>P68-PWR+GPU CORE</b>			
	<b>LA-F541P</b>			
	File	Size		Document Number
				0.10
Date: Wednesday, June 06, 2018      Sheet 68 of 74				

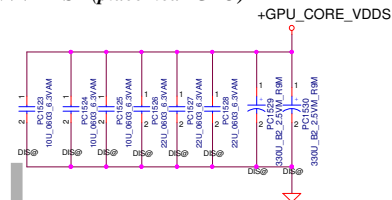
Vmax=1.3V  
Vmin=0.3V  
Vboot=0.8V

```
+GPU_CORE_VDDSD
TDC 12A
Peak Current 16A
OCP current 21A
DCR 0.98mohm +/- 5%
```

	MIN	MAX
H/S Rds(on)	3.7mohm	4.5mohm
L/S Rds(on)	1.5mohm	1.9mohm



**NVVDDS** (*place near GPU*)



Under:  
4.7U\_0603\_6.3VAK \*6  
1U\_0402\_6.3VAK \*4

Near:  
10U\_0603\_6.3VAM \*3  
22U\_0603\_6.3VAM \*3  
330u\*2

- VGA\_CORE controller(43.1), Support component(43.2)
- VGA\_CORE Drivers (43.3), GPU Core Output CAP (43.9)

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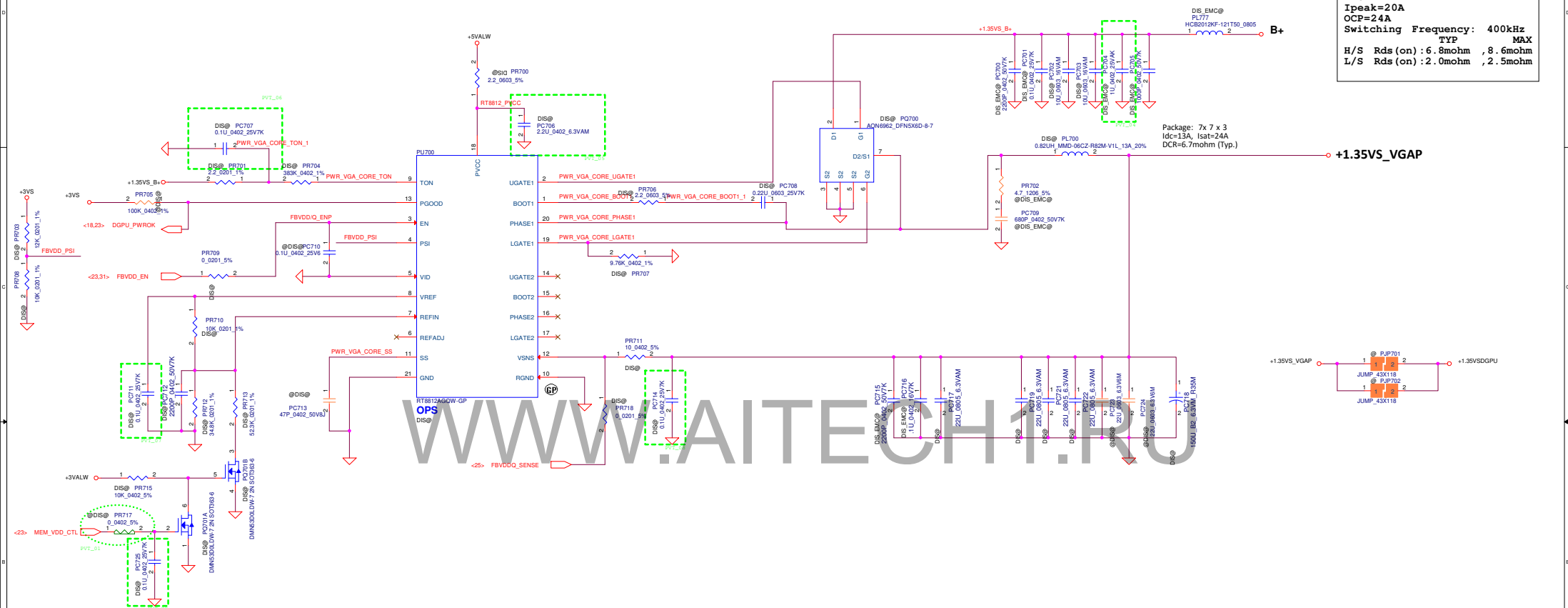
### P69-PWR-+GPU CORE VDDS

Number  
LA-F541P

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	<b>LA-F541P</b>	0.1(000)
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```
for dGPU SKU
@DIS@ : Nopop Component
DIS@: POP for dGPU SKU
```



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				Document Number	01000
				LA-E994P	
				Date: Wednesday, Jun 01, 2018	Sheet 71 of 74

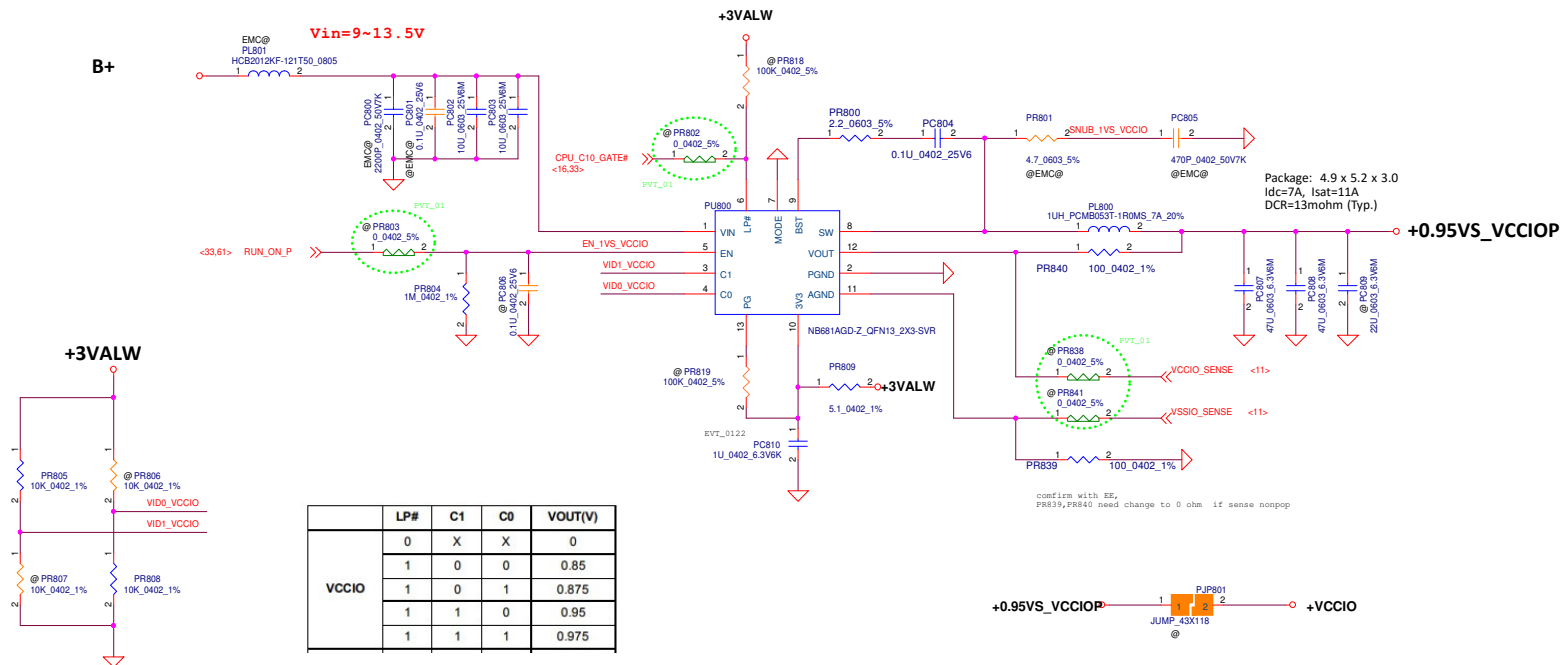
2.5V\_MEM controller(35.13), Support component(35.14)

```
+2.5V_MEM
TDC 0.86A
Peak Current 1A
OCP Current 1.46A
```



Security Classification	Compal Secret Data			<b>Compal Electronics, Inc.</b>		
Issued Date	2017/06/21	Deciphered Date	2027/06/21	Title <b>P72-PWR +2.5V MEM(RT9059GSP)</b>		
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+0.95VS\_VCCIO  
TDC 3.9A  
Peak Current 5.5 A  
OCP Current 6.6 A Fix by IC  
TYP MAX

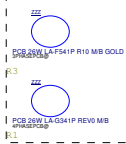
WWW.AITECH1.RU

Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	NA	NA	2014/12/12	EE	NA	NA	X01
2				EE			X01
3				EE			X01
4				EE			X01
5				EE			X01
6				EE			X01
7				EE			X01
8				EE			X01
9				EE			X01
10				EE			X01
11				EE			X01
12				EE			X01
13				EE			X01
14				EE			X01
15				EE			X01
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17				EE			X01
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41				EE			

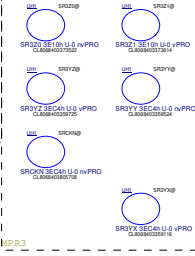
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Project Code :  
File Name :

PCB



CPU



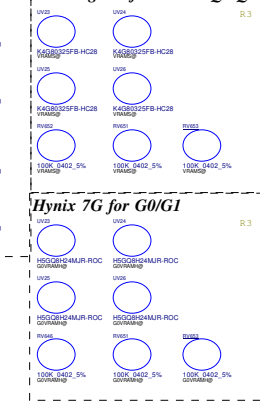
PCH



GPU



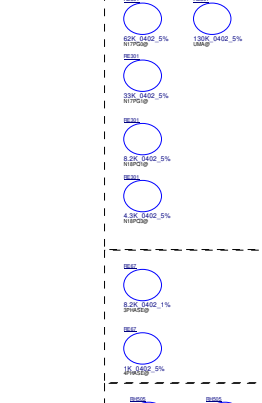
Samsung 7G for G0/G1/Q1/Q3



Micron 7G for G0/G1/Q1/Q3



Hynix 7G for G0/G1



RE301CE3319

RE301CE3319	CONFIG
240K 4700p	
130K 4700p	UMA
62K 4700p	N17P-G0
33K 4700p	N17P-G1
8.2K 4700p	N18P-Q1
4.3K 4700p	N18P-Q3
2K 4700p	
1K 4700p	

RE67	CE51	REV	PHASE
240K 4700p	X00	EVT	
130K 4700p	X01	PRE DVT	
62K 4700p	X02	DVT1	
33K 4700p	X03	DVT2	
8.2K 4700p	A00	PVT	
4.3K 4700p	X00 4P	I9 EVT	
2K 4700p	X01 4P	I9 DVT	
1K 4700p	A00 4P	I9 PVT	

TLS CONFIDENTIALITY  
HIGH(4.7K)  
LOW(DEFAULT)(130K)  
WDS 25k internal pull-down

DRAM Option

SDP  
MICRON 8G/2400

SDP  
HYNIX 8G/2400

SDP  
SAMSUNG 8G/2400

DDP  
MICRON 16G/2400

DDP  
HYNIX 16G/2400

DDP  
SAMSUNG 16G/2400

DRAM Config Option

MEM\_CONFIG1 MEM\_CONFIG2 MEM\_CONFIG3 MEM\_CONFIG4

DRAM SDP / DDP Option

R\_COMP

X76

X7674531L07

X7674531L09

X7674531L08

X7674531L10

X7674531L15

X7674531L11

DELL CONFIDENTIAL/PROPRIETARY

Security Classification	Compal Secret Data	Rev	Compal Electronics, Inc.
Issued Date	20170407	20161201	
BOM Option			
LA-G341P			

